

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
1 May 2003 (01.05.2003)

PCT

(10) International Publication Number
WO 03/036374 A1

- (51) International Patent Classification⁷: G02F 1/1343
- (21) International Application Number: PCT/KR02/00334
- (22) International Filing Date: 27 February 2002 (27.02.2002)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
2001/59637 26 September 2001 (26.09.2001) KR
2001/77838 10 December 2001 (10.12.2001) KR
- (71) Applicant (for all designated States except US): SAM-SUNG ELECTRONICS CO., LTD. [KR/KR]; 416, Maetan-dong, Paldal-ku, Suwon-city 442-370, Kyungki-do (KR).
- (72) Inventors; and
(75) Inventors/Applicants (for US only): LEE, Chang-Hun

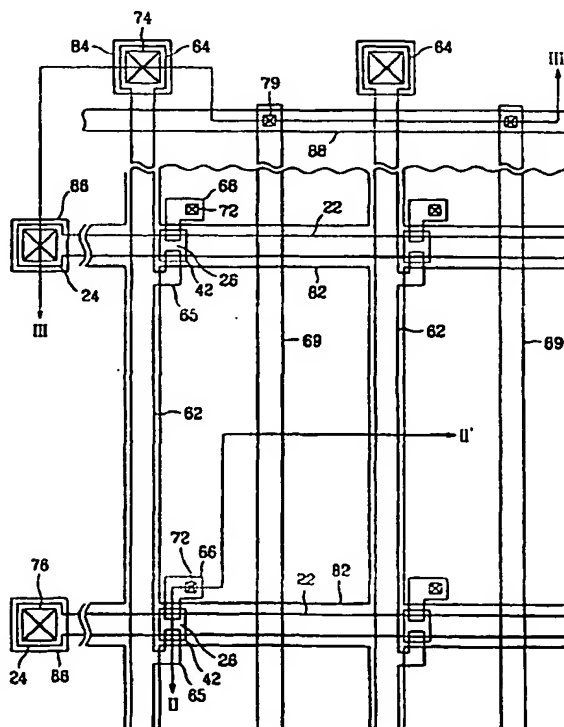
[KR/KR]; Shinnamushil Ssangyong Apt. 542-203, Young-tong-dong, Paldal-ku, Suwon-city 442-470, Kyungki-do (KR). KIM, Nam-Hung [KR/KR]; 990-16, Young-tong-dong, Paldal-ku, Suwon-city 442-813, Kyungki-do (KR). CHANG, Hak-Sun [KR/KR]; Gaenari Apt. 1-104, Yoksam 2-dong, Kangnam-ku, Seoul 135-795 (KR). LYU, Jae-Jin [KR/KR]; 692, Yangbyeol 1-ri, Opo-myeon, Kwangju-kun, Kyungki-do 464-896 (KR).

(74) Agent: YOU ME PATENT & LAW FIRM; Teheran Bldg., 825-33, Yoksam-dong, Kangnam-ku, Seoul 135-080 (KR).

(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

[Continued on next page]

(54) Title: THIN FILM TRANSISTOR ARRAY PANEL FOR LIQUID CRYSTAL DISPLAY AND METHOD FOR MANUFACTURING THE SAME



(57) Abstract: In a method of fabricating a liquid crystal display, an insulating layer for storage capacitors is reduced in thickness to increase the storage capacity while maintaining the aperture ratio in a stable manner. A thin film transistor array panel for the liquid crystal display includes an insulating substrate, and a gate line assembly and a storage capacitor line assembly formed on the insulating substrate. The gate line assembly has gate lines and gate electrodes. A gate insulating layer covers the gate line assembly and the storage capacitor line assembly. A semiconductor pattern is formed on the gate insulating layer. A data line assembly and storage capacitor conductive patterns are formed on the gate insulating layer overlaid with the semiconductor pattern. The data line assembly has data lines, source electrodes and drain electrodes. The storage capacitor conductive patterns are partially overlapped with the storage capacitor line assembly to thereby form first storage capacitors. A passivation layer covers the data line assembly, the storage capacitor conductive patterns and the semiconductor pattern. First and second contact holes are formed at the passivation layer while exposing the drain electrodes and the storage capacitor conductive patterns. Pixel electrodes are formed on the passivation layer while being connected to the drain electrodes and the storage capacitor conductive patterns through the first and the second contact holes. The pixel electrodes form second storage capacitors in association with parts of the storage capacitor line assembly.



WO 03/036374 A1



(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

THIN FILM TRANSISTOR ARRAY PANEL FOR LIQUID CRYSTAL
DISPLAY AND METHOD FOR MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

5 (a) **Field of the Invention**

The present invention relates to a thin film transistor array panel for a liquid crystal display, and a method for manufacturing the same.

(b) **Description of the Related Art**

Generally, a liquid crystal display has two substrates with electrodes,
10 and a liquid crystal layer sandwiched between the two substrates. Voltages are applied to the electrodes so that the liquid crystal molecules in the liquid crystal layer are re-oriented to thereby control the light transmission. The electrodes may be all formed at one of the substrates. One of the substrates is called the "thin film transistor array panel", and the other is
15 called the "color filter substrate."

The thin film transistor array panel has a plurality of gate lines, data lines crossing over the gate lines while defining pixel regions, thin film transistors formed at the respective pixel regions while being electrically connected to the gate and the data lines, and pixel electrodes electrically
20 connected to the thin film transistors.

Storage capacitors are formed at the thin film transistor array panel to keep the voltage applied to the liquid crystal disposed between the two substrates in a stable manner. For that purpose, a storage capacitor line assembly is formed at the same layer as the gate lines such that it is

overlapped with the pixel electrodes to thereby form storage capacitors. Meanwhile, the electrostatic capacitance of the storage capacitors should be increased to enhance the brightness of the display device or to make rapid response speed thereof. In this connection, it is necessary to enlarge the
5 area of the storage capacitor line assembly, but this causes decreased aperture or opening ratio.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a thin film transistor array panel for a liquid crystal display which involves storage capacitors with
10 increased electrostatic capacitance while bearing a reasonable aperture ratio.

This and other objects may be achieved by a thin film transistor array panel for a liquid crystal display where the storage capacitor line assembly is formed at the same layer as the data lines, or the thickness of the insulating layer for the storage capacitors is minimized.

15 According to one aspect of the present invention, the thin film transistor array panel includes an insulating substrate, and a gate line assembly formed on the insulating substrate and including gate lines, and gate electrodes. A gate insulating layer covers the gate line assembly. A semiconductor pattern is formed on the gate insulating layer. A data line
20 assembly is formed on the gate insulating layer overlaid with the semiconductor pattern. The data line assembly has data lines crossing over the gate lines, source electrodes connected to the data lines and the semiconductor pattern, and drain electrodes facing the source electrodes and connected to the semiconductor pattern. Storage capacitor electrode lines

are formed between the neighboring data lines while crossing over the gate lines. A passivation layer covers the data line assembly, the storage capacitor electrode lines and the semiconductor pattern while bearing contact holes exposing the drain electrodes. Pixel electrodes are formed on the
5 passivation layer while being connected to the drain electrodes through the contact holes. The pixel electrodes are overlapped with the storage capacitor electrode lines.

The thin film transistor array panel may further include a common interconnection line commonly interconnecting the storage capacitor
10 electrode lines. The common interconnection line may be formed with the same material as the pixel electrodes or the gate lines while crossing over the data lines in an insulated manner.

The passivation layer has a plurality of contact holes exposing the storage capacitor electrode lines, and the common interconnection line is
15 connected to the storage capacitor electrode lines through the contact holes. A subsidiary interconnection line may be connected to the storage capacitor electrode lines. The storage capacitor electrode lines and the subsidiary interconnection line are formed with the same material.

Gate pads are formed at one-sided end portions of the gate lines,
20 and data pads are formed at one-sided end portions of the data lines. First contact holes are formed at the passivation layer and the gate insulating layer while exposing the gate pads, and second contact holes are formed at the passivation layer while exposing the data pads. Subsidiary gate and data pads are connected to the gate and the data pads through the first and
25 the second contact holes.

In addition to the above-structured thin film transistor array panel, the liquid crystal display includes a counter substrate facing the thin film transistor array panel, and a liquid crystal layer sandwiched between the thin film transistor array panel and the counter panel. The liquid crystal display
5 has storage capacitors with an electrostatic capacitance greater than the electrostatic capacitance of the liquid crystal capacitor having the liquid crystal layer by 90% or more.

According to another aspect of the present invention, the thin film transistor array panel includes an insulating substrate, and a gate line
10 assembly and a storage capacitor line assembly formed on the insulating substrate. The gate line assembly has gate lines and gate electrodes. A gate insulating layer covers the gate line assembly and the storage capacitor line assembly. A semiconductor pattern is formed on the gate insulating layer. A data line assembly and storage capacitor conductive patterns are
15 formed on the gate insulating layer overlaid with the semiconductor pattern. The data line assembly has data lines, source electrodes and drain electrodes. The storage capacitor conductive patterns are partially overlapped with the storage capacitor line assembly to thereby form first storage capacitors. A passivation layer covers the data line assembly, the
20 storage capacitor conductive patterns and the semiconductor pattern. First and second contact holes are formed at the passivation layer while exposing the drain electrodes and the storage capacitor conductive patterns, respectively. Pixel electrodes are formed on the passivation layer while being connected to the drain electrodes and the storage capacitor conductive
25 patterns through the first and the second contact holes. The pixel

electrodes form second storage capacitors in association with parts of the storage capacitor line assembly.

The storage capacitor line assembly has storage capacitor electrode lines proceeding parallel to the gate lines, and storage capacitor electrode patterns connected to the storage capacitor electrode lines. The storage capacitor electrode patterns are overlapped with the storage capacitor conductive patterns to thereby form the first storage capacitors, and the storage capacitor electrode lines are overlapped with the pixel electrodes to thereby form the second storage capacitors.

10 The storage capacitor electrode patterns are formed within pixel regions defined by the gate lines and the data lines. The storage capacitor electrode patterns are formed with a bar shape along the data lines while being overlapped with peripheral portions of the pixel electrodes.

In addition to the above-structured thin film transistor array panel, the liquid crystal display includes a counter substrate facing the thin film transistor array panel, and a liquid crystal layer sandwiched between the thin film transistor array panel and the counter panel. The first and the second storage capacitors have an electrostatic capacitance greater than the electrostatic capacitance of the liquid crystal layer by 90% or more.

20 According to still another aspect of the present invention, the thin film transistor array panel includes an insulating substrate, and a gate line assembly formed on the insulating substrate. The gate line assembly has first gate lines, gate electrodes connected to the first gate lines, and second gate lines spaced apart from the first gate lines with a predetermined distance. A gate insulating layer covers the gate line assembly. A

25

semiconductor pattern is formed on the gate insulating layer while being overlapped with the gate electrodes. A data line assembly and storage capacitor conductive patterns are formed on the gate insulating layer overlaid with the semiconductor pattern. The data line assembly has data
5 lines crossing over the first and the second gate lines, source electrodes and drain electrodes. The storage capacitor conductive patterns are partially overlapped with the second gate lines to thereby form first storage capacitors. A passivation layer covers the data line assembly, the storage capacitor conductive patterns and the semiconductor pattern. First and second
10 contact holes are formed at the passivation layer while exposing the drain electrodes and the storage capacitor conductive patterns, respectively. Pixel electrodes are formed at the passivation layer while being connected to the drain electrodes and the storage capacitor conductive patterns through the first and the second contact holes. The pixel electrodes are partially
15 overlapped with the second gate lines to thereby form second storage capacitors.

In addition to the above-structured thin film transistor array panel, the liquid crystal display includes a counter substrate facing the thin film transistor array panel, and a liquid crystal layer sandwiched between the thin
20 film transistor array panel and the counter panel. The first and the second storage capacitors have an electrostatic capacitance greater than the electrostatic capacitance of the liquid crystal layer by 90% or more.

According to still another aspect of the present invention, the thin film transistor array panel includes an insulating substrate, and a gate line
25 assembly and storage capacitor electrode lines formed on the insulating

substrate. The gate line assembly has gate lines and gate electrodes. A gate insulating layer covers the gate line assembly and the storage capacitor electrode lines. First contact holes are formed at the gate insulating layer while exposing the storage capacitor electrode lines. A semiconductor pattern is formed on the gate insulating layer while being overlapped with the gate electrodes. A data line assembly and storage capacitor conductive patterns are formed on the gate insulating layer overlaid with the semiconductor pattern. The data line assembly has data lines, source electrodes and drain electrodes. The storage capacitor conductive patterns are connected to the storage capacitor electrode lines through the first contact holes. A passivation layer covers the data line assembly, the storage capacitor conductive patterns and the semiconductor pattern. Second contact holes are formed at the passivation layer while exposing the drain electrodes. Pixel electrodes are formed at the passivation layer while being connected to the drain electrodes through the second contact holes. The pixel electrodes are overlapped with the storage capacitor conductive patterns to thereby form first storage capacitors while being partially overlapped with the storage capacitor electrode lines to thereby form second storage capacitors.

The storage capacitor electrode lines proceed parallel to the gate lines, and the storage capacitor conductive patterns are overlapped with the storage capacitor electrode lines. The storage capacitor conductive patterns are formed within pixel regions defined by the gate lines and the data lines. The storage capacitor electrode patterns are formed with a bar shape along the data lines while being overlapped with peripheral portions of

the pixel electrodes.

In addition to the above-structured thin film transistor array panel, the liquid crystal display includes a counter substrate facing the thin film transistor array panel, and a liquid crystal layer sandwiched between the thin film transistor array panel and the counter panel. The first and the second storage capacitors have an electrostatic capacitance greater than the electrostatic capacitance of the liquid crystal layer by 90% or more.

According to still another aspect of the present invention, the thin film transistor array panel includes an insulating substrate, and a gate line assembly formed on the insulating substrate. The gate line assembly has first gate lines, gate electrodes connected to the first gate lines, and second gate lines spaced apart from the first gate lines with a predetermined distance. A gate insulating layer covers the gate line assembly. First contact holes are formed at the gate insulating layer while partially exposing the second gate lines. A semiconductor pattern is formed on the gate insulating layer while being overlapped with the gate electrodes. A data line assembly and storage capacitor conductive patterns are formed on the gate insulating layer overlaid with the semiconductor pattern. The data line assembly has data lines crossing over the first and the second gate lines, source electrodes and drain electrodes. The storage capacitor conductive patterns are connected to the second gate lines through the first contact holes. A passivation layer covers the data line assembly, the storage capacitor conductive patterns and the semiconductor pattern. Second contact holes are formed at the passivation layer while exposing the drain electrodes. Pixel electrodes are formed at the passivation layer while being

connected to the drain electrodes through the second contact holes. The pixel electrodes are overlapped with the storage capacitor conductive patterns to thereby form first storage capacitors while being partially overlapped with the second gate lines to thereby form second storage
5 capacitors.

In addition to the above-structured thin film transistor array panel, the liquid crystal display includes a counter substrate facing the thin film transistor array panel, and a liquid crystal layer sandwiched between the thin film transistor array panel and the counter panel. The first and the second
10 storage capacitors have an electrostatic capacitance greater than the electrostatic capacitance of the liquid crystal layer by 90% or more.

According to still another aspect of the present invention, in a method of fabricating a thin film transistor array panel, a gate line assembly and a storage capacitor line assembly are formed on an insulating substrate such
15 that the gate line assembly has gate lines and gate electrodes. A gate insulating layer is formed on the substrate such that it covers the gate line assembly and the storage capacitor line assembly. A semiconductor pattern is formed on the gate insulating layer. A data line assembly and storage capacitor conductive patterns are formed on the gate insulating layer overlaid
20 with the semiconductor pattern such that the data line assembly has data lines, source electrodes and drain electrodes, and the storage capacitor conductive patterns are partially overlapped with the storage capacitor line assembly to thereby form first storage capacitors. A passivation layer is formed on the substrate such that it covers the data line assembly, the
25 storage capacitor conductive patterns and the semiconductor pattern. First

and second contact holes are formed at the passivation layer such that they expose the drain electrodes and the storage capacitor conductive patterns, respectively. Pixel electrodes are formed on the passivation layer such that they are connected to the drain electrodes and the storage capacitor
5 conductive patterns through the first and the second contact holes while forming second storage capacitors in association with parts of the storage capacitor lines assembly.

The storage capacitor line assembly has storage capacitor electrode lines proceeding parallel to the gate lines, and storage capacitor electrode
10 patterns connected to the storage capacitor electrode lines.

According to still another aspect of the present invention, in a method of fabricating a thin film transistor array panel, a gate line assembly is formed on an insulating substrate such that it has first gate lines, gate electrodes connected to the first gate lines, and second gate lines spaced apart from the
15 first gate lines with a predetermined distance while proceeding parallel to the first gate lines. A gate insulating layer is formed on the substrate such that it covers the gate line assembly. A semiconductor pattern is formed on the gate insulating layer such that it is overlapped with the gate electrodes. A data line assembly and storage capacitor conductive patterns are formed on
20 the gate insulating layer overlaid with the semiconductor pattern such that the data line assembly has data lines crossing over the first and the second gate lines, source electrodes and drain electrodes, and the storage capacitor conductive patterns are partially overlapped with the second gate lines to thereby form first storage capacitors. A passivation layer is formed on the
25 substrate such that it covers the data line assembly, the storage capacitor

conductive patterns and the semiconductor pattern. First and second contact holes are formed at the passivation layer such that the first and the second contact holes expose the drain electrodes and the storage capacitor conductive patterns, respectively. Pixel electrodes are formed on the passivation layer such that they are connected to the drain electrodes and the storage capacitor conductive patterns through the first and the second contact holes while forming second storage capacitors in association with parts of the second gate lines.

According to still another aspect of the present invention, in a method of fabricating a thin film transistor array panel, a gate line assembly and storage capacitor electrode lines are formed on an insulating substrate such that the gate line assembly has gate lines and gate electrodes. A gate insulating layer is formed on the substrate such that it covers the gate line assembly and the storage capacitor electrode lines. First contact holes are formed at the gate insulating layer such that they expose the storage capacitor electrode lines. A semiconductor pattern is formed on the gate insulating layer such that it is overlapped with the gate electrodes. A data line assembly and storage capacitor conductive patterns are formed on the gate insulating layer overlaid with the semiconductor pattern such that the data line assembly has data lines, source electrodes and drain electrodes, and the storage capacitor conductive patterns are connected to the storage capacitor electrode lines through the first contact holes. A passivation layer is formed on the substrate such that it covers the data line assembly, the storage capacitor conductive patterns and the semiconductor pattern. Second contact holes are formed at the passivation layer such that they

expose the drain electrodes. Pixel electrodes are formed on the passivation layer such that they are connected to the drain electrodes through the second contact holes. The pixel electrodes are overlapped with the storage capacitor conductive patterns to thereby form first storage capacitors while
5 being partially overlapped with the storage capacitor electrode lines to thereby form second storage capacitors.

According to still another aspect of the present invention, in a method of fabricating a thin film transistor array panel, a gate line assembly is formed on an insulating substrate such that it has first gate lines, gate electrodes
10 connected to the first gate lines, and second gate lines spaced apart from the first gate lines with a predetermined distance while proceeding parallel to the first gate lines. A gate insulating layer is formed on the substrate such that it covers the gate line assembly. First contact holes are formed at the gate insulating layer such that they partially expose the second gate lines. A
15 semiconductor pattern is formed on the gate insulating layer such that it is overlapped with the gate electrodes. A data line assembly and storage capacitor conductive patterns are formed on the gate insulating layer overlaid with the semiconductor pattern such that the data line assembly has data lines crossing over the first and the second gate lines, source electrodes and
20 drain electrodes, and the storage capacitor conductive patterns are connected to the second gate lines through the first contact holes. A passivation layer is formed on the substrate such that it covers the data line assembly, the storage capacitor conductive patterns and the semiconductor pattern. Second contact holes are formed at the passivation layer such that
25 they expose the drain electrodes. Pixel electrodes are formed on the

passivation layer such that they are connected to the drain electrodes through the second contact holes. The pixel electrodes are overlapped with the storage capacitor conductive patterns to thereby form first storage capacitors while being partially overlapped with the second gate lines to
5 thereby form second storage capacitors.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete appreciation of the invention, and many of the attendant advantages thereof, will be readily apparent as the same becomes better understood by reference to the following detailed description when
10 considered in conjunction with the accompanying drawings in which like reference symbols indicate the same or the similar components, wherein:

Fig. 1 is a plan view of a thin film transistor array panel according to a first preferred embodiment of the present invention;

Figs. 2 and 3 are cross sectional views of the thin film transistor array
15 panel taken along the II-II' line and the III-III' line of Fig. 1;

Fig. 4 illustrates the layout of gate lines, data lines and storage capacitor electrode lines at the thin film transistor array panel shown in Fig. 1;

Fig. 5A illustrates the first step of fabricating the thin film transistor array panel shown in Fig. 1;

20 Figs. 5B and 5C are cross sectional views of the thin film transistor array panel taken along the VB-VB' line and the VC-VC' line of Fig. 5A;

Fig. 6A illustrates the step of fabricating the thin film transistor array panel following the step illustrated in Fig. 5A;

Figs. 6B and 6C are cross sectional views of the thin film transistor

array panel taken long the VIB-VIB' line and the VIC-VIC' line of Fig. 6A;

Fig. 7A illustrates the step of fabricating the thin film transistor array panel following the step illustrated in Fig. 6A;

Figs. 7B and 7C are cross sectional views of the thin film transistor array panel taken long the VIIB-VIIB' line and the VIIC-VIIC' line of Fig. 7A;

Fig. 8 is a plan view of a thin film transistor array panel according to a second preferred embodiment of the present invention;

Fig. 9 is a cross sectional view of the thin film transistor array panel taken along the IX-IX' line of Fig. 8;

Fig. 10A illustrates the first step of fabricating the thin film transistor array panel shown in Fig. 8;

Figs. 10B is a cross sectional view of the thin film transistor array panel taken long the XBb-XB' line of Fig. 10A;

Fig. 11A illustrates the step of fabricating the thin film transistor array panel following the step illustrated in Fig. 10A;

Fig. 11B is a cross sectional view of the thin film transistor array panel taken long the XIB-XIB' line of Fig. 11A;

Fig. 12A illustrates the step of fabricating the thin film transistor array panel following the step illustrated in Fig. 11A;

Fig. 12B is a cross sectional view of the thin film transistor array panel taken long the XIIB-XIIB' line of Fig. 12A;

Fig. 13A illustrates the step of fabricating the thin film transistor array panel following the step illustrated in Fig. 12A;

Fig. 13B is a cross sectional view of the thin film transistor array panel taken long the XIIIB-XIIIB' line of Fig. 13A;

Fig. 14 is a plan view of a thin film transistor array panel according to a third preferred embodiment of the present invention;

Fig. 15 is a cross sectional view of the thin film transistor array panel taken along the XV-XV' line of Fig. 14;

5 Fig. 16 is a plan view of a thin film transistor array panel according to a fourth preferred embodiment of the present invention;

Fig. 17 is a cross sectional view of the thin film transistor array panel taken long the XVII-XVII' line of Fig. 16;

10 Fig. 18 is a plan view of a thin film transistor array panel according to a fifth preferred embodiment of the present invention;

Fig. 19 is a cross sectional view of the thin film transistor array panel taken long the XIX-XIX' line of Fig. 18;

Fig. 20A illustrates the first step of fabricating the thin film transistor array panel shown in Fig. 18;

15 Fig. 20B is a cross sectional view of the thin film transistor array panel taken long the XXB-XXB' line of Fig. 20A;

Fig. 21A illustrates the step of fabricating the thin film transistor array panel following the step illustrated in Fig. 20A;

20 Fig. 21B is a cross sectional view of the thin film transistor array panel taken long the XXIB-XXIB' line of Fig. 21A;

Fig. 22A illustrates the step of fabricating the thin film transistor array panel following the step illustrated in Fig. 21A;

Fig. 22B is a cross sectional view of the thin film transistor array panel taken long the XXIIB-XXIIB' line of Fig. 22A;

25 Fig. 23A illustrates the step of fabricating the thin film transistor array

panel following the step illustrated in Fig. 22A;

Fig. 23B is a cross sectional view of the thin film transistor array panel taken long the XXIIIB-XXIIIB' line of Fig. 23A;

Fig. 24A illustrates the step of fabricating the thin film transistor array panel following the step illustrated in Fig. 23A;

Fig. 24B is a cross sectional view of the thin film transistor array panel taken long the XXIVB-XXIVB' line of Fig. 24A;

Fig. 25 is a plan view of a thin film transistor array panel according to a sixth preferred embodiment of the present invention;

Fig. 26 is a cross sectional view of the thin film transistor array panel taken long the XXVI-XXVI' line of Fig. 25;

Fig. 27 is a plan view of a thin film transistor array panel according to a seventh preferred embodiment of the present invention;

Fig. 28 is a cross sectional view of the thin film transistor array panel taken long the XXVIII-XXVIII' line of Fig. 27; and

Fig. 29 illustrates a waveform curve of the response speed in a liquid crystal display.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of this invention will be explained with reference to the accompanying drawings.

Fig. 1 is a plan view of a thin film transistor array panel for a liquid crystal display according to a first preferred embodiment of the present invention, and Figs. 2 and 3 are cross sectional views of the thin film transistor array panel taken along the II-II' line and the III-III' line of Fig. 1.

A gate line assembly is formed on an insulating substrate 10 with a conductive material such as aluminum, aluminum alloy, chrome, chrome alloy, molybdenum, molybdenum alloy, chrome nitride, and molybdenum nitride while bearing a thickness of 1000-3500 Å. The gate line assembly
5 includes gate lines 22 proceeding in the horizontal direction, gate pads 24 connected to the one-sided ends of the gate lines 22 while electrically contacting external driving circuits (not shown), and gate electrodes 26 being parts of the gate lines 22 while forming thin film transistors with other electrode components.

10 The gate line assembly may have a multiple-layered structure where one layer is formed with a low resistance metallic material, and the other layer with a material bearing a good contact characteristic with other materials.

A gate insulating layer 30 with a thickness of 2,500-4,500 Å is
15 formed on the insulating substrate 10 with silicon nitride or silicon oxide while covering the gate line assembly.

A semiconductor pattern 42 with a thickness of 800-1500 Å is formed on the gate insulating layer 30 with amorphous silicon while being overlapped with the gate electrodes 26. Ohmic contact patterns 55 and 56
20 with a thickness of 500-800 Å are formed on the semiconductor pattern 42 with amorphous silicon where n type impurities are doped at high concentration.

A data line assembly and storage capacitor electrode lines 69 are formed on the ohmic contact patterns 55 and 56, and the gate insulating

layer 30 with a conductive material such as aluminum, aluminum alloy, chrome, chrome alloy, molybdenum, molybdenum alloy, chrome nitride and molybdenum nitride while bearing a thickness of 500-3500 Å. The data line assembly includes data lines 62 proceeding in the vertical direction while
5 crossing over the gate lines 22 to define pixel regions, data pads 64 connected to the one-sided ends of the data lines 62 while electrically contacting external driving circuits, source electrodes 65 connected to the data lines 62 while being extended over the ohmic contact pattern 55, and drain electrodes 66 facing the source electrodes 65 while being placed over
10 the other ohmic contact pattern 56. The drain electrodes 66 are extended over the gate insulating layer 30 within the pixel regions.

The storage capacity electrode lines 69 are placed at the same plane as the data line assembly while proceeding in the vertical direction such that they are alternately arranged with the data lines 62. The storage capacity
15 electrode lines 69 are overlapped with pixel electrodes 82 to thereby form storage capacitors.

The data line assembly may have a multiple-layered structure where at least one layer is formed with a low resistance metallic material.

A passivation layer 70 covers the data line assembly, the storage
20 capacitor electrode lines 69 and the semiconductor pattern 42 while bearing a thickness of 500-2000 Å. The passivation layer 70 is formed with an insulating material such as silicon nitride and silicon oxide.

First and second contact holes 72 and 74 are formed at the passivation layer 70 while exposing the drain electrodes 66 and the data

pads 64. Third contact holes 76 are formed at the passivation layer 70 while exposing the gate pads 24 together with the gate insulating layer 30. Furthermore, fourth contact holes 79 are formed at the passivation layer 70 while exposing the end portions of the storage capacitor electrode lines 69 sided with the data pads 64.

Pixel electrodes 82 are formed on the passivation layer 70 to receive picture signals and generate electric fields together with a common electrode (not shown) of the counter panel. The pixel electrodes 82 are electrically connected to the drain electrodes 66 through the first contact holes 72.

10 The pixel electrodes 82 are overlapped with the storage capacitor electrode lines 69 while interposing the passivation layer 70 to thereby form storage capacitors. As the passivation layer 70 disposed between the pixel electrodes 82 and the storage capacitor electrode lines 69 bears a thin thickness, the resulting storage capacitors bear a great electrostatic
15 capacitance even when the storage capacitor electrode lines 69 bear a narrow width.

Subsidiary data pads 84 and subsidiary gate pads 86 are formed on the passivation layer 70 while being connected to the data pads 64 and the gate pads 24 through the second and the third contact holes 74 and 76.
20 Furthermore, a common interconnection line 88 is formed external to the display area while proceeding parallel to the gate lines 22. The display area refers to the sum of the pixel regions. The common interconnection line 88 interconnects all of the storage capacitor electrode lines 69 through the fourth contact holes 79.

25 The pixel electrodes 82, the subsidiary data pads 84, the subsidiary

gate pads 86 and the common interconnection line 88 are formed at the same plane with a transparent conductive material such as ITO and IZO.

The common interconnection line 88 may be formed with the same material as the gate line assembly during the process of forming the gate line assembly. In this case, a plurality of contact holes are formed at the gate insulating layer 30 while exposing the common interconnection line 88. The plurality of storage capacitor electrode lines 69 contact the common interconnection line 88 through the contact holes formed at the gate insulating layer 30.

Fig. 4 illustrates the arrangement of the gate lines, the data lines and the storage capacitor electrode lines at the thin film transistor array panel shown in Fig. 1.

As shown in Fig. 4, the plurality of gate lines 22 proceed in the horizontal direction parallel to each other, and the plurality of data lines 62 proceed in the vertical direction parallel to each other. The data lines 62 cross over the gate lines 22 while defining the pixel regions. The display area 110 refers to the sum of the pixel regions.

The one-sided end portions of the data lines 62 being the data pads are electrically connected to data driving circuits 300 to receive data signals from them. Similarly, the one-sided end portions of the gate lines 22 being the gate pads are electrically connected to gate driving circuits (not shown) to receive gate signals from them.

The storage capacitor electrode lines 69 are alternately arranged with the data lines 62. The storage capacitor electrode lines 69 are connected to each other by way of a subsidiary interconnection line 61

placed external to the display area 110. It is preferable that the storage capacitor electrode lines 69 and the subsidiary interconnection line 61 are formed with the same material while being commonly interconnected.

The common interconnection line 88 is placed at the ends of the storage capacitor electrode lines 69 sided with the data driving circuits while interconnecting all of the storage capacitor electrode lines 69. It is preferable that the common interconnection line 88 is formed with the same material as the pixel electrodes 82 or the gate line assembly. This is to prevent the common interconnection line 88 from being short circuited with the portions of the data lines 62 connected to the data driving circuits 300 external to the display area 110.

The storage capacitor electrode lines 69 are electrically connected to the data driving circuits 300 to receive common electrode voltages from them.

A method of fabricating the thin film transistor array panel will be now explained with reference to Figs. 5A to 7C as well as Figs. 1 to 4.

As shown in Figs. 5A to 5C, a gate line assembly layer is deposited onto an insulating substrate 10, and patterned through photolithography to thereby form a gate line assembly. The gate line assembly includes gate lines 22, gate pads 24, and gate electrodes 26.

Thereafter, a gate insulating layer 30 based on an insulating material such as silicon nitride is deposited onto the insulating substrate 10 such that it covers the gate line assembly.

An amorphous silicon layer and a conductive type impurities-doped amorphous silicon layer are sequentially deposited onto the gate insulating layer 30, and patterned through photolithography to thereby form a

semiconductor pattern 42 and an ohmic contact pattern 52.

As shown in Figs. 6A to 6C, a metallic layer is deposited onto the entire surface of the substrate, and patterned through photolithography to thereby form a data line assembly and storage capacitor electrode lines 69.

5 The data line assembly includes data lines 62, data pads 64, source electrodes 65, and drain electrodes 66. The storage capacitor electrode lines 69 are alternately arranged with the data lines 62.

The ohmic contact pattern 52 is etched using the source electrode 65 and the drain electrode 66 as a mask to thereby separate it into a first portion
10 55 contacting the source electrode 65, and a second portion 56 contacting the drain electrode 66.

As shown in Figs. 7A to 7C, a passivation layer 70 covers the data line assembly, the storage capacitor electrode lines 69, and the semiconductor pattern 42. The passivation layer 70 is formed with silicon
15 nitride while bearing a thin thickness. In consideration of the electrostatic capacitance of the storage capacitors to be formed, it is preferable that the thickness of the passivation layer 70 is controlled in an appropriate manner.

The passivation layer 70 and the gate insulating layer 30 are patterned through photolithography to thereby form first to fourth contact
20 holes 72, 74, 76 and 79.

As shown in Figs. 1 to 3, a transparent conductive layer based on ITO or IZO is deposited onto the entire surface of the substrate 10.

The transparent conductive layer is patterned through photolithography to thereby form pixel electrodes 82, subsidiary data pads 84,
25 subsidiary gate pads 86, and a common interconnection line 88. The pixel

electrodes 82 are connected to the drain electrodes 66 through the first contact holes 72. The subsidiary data and gate pads 84 and 86 are connected to the data and gate pads 64 and 24 through the second and the third contact holes 74 and 76. The common interconnection line 88
5 interconnects all of the storage capacitor electrode lines 69 through the fourth contact holes 79.

The common interconnection line 88 may be formed with the same material as the gate line assembly. For that purpose, the common interconnection line is formed during the process of forming the gate line
10 assembly while being followed by the formation of the gate insulating layer 30. A plurality of contact holes exposing the common interconnection line are then formed at the gate insulating layer 30. The storage capacitor electrode lines 69 are formed during the process of forming the data line assembly. In this process, the storage capacitor electrode lines 69 are connected to the
15 common interconnection line through the contact holes.

As described above, the storage capacitor electrode lines are formed at the same plane as the data lines such that they are overlapped with the pixel electrodes while interposing the passivation layer bearing a thin thickness to thereby form storage capacitors.

20 Alternatively, the storage capacitors may be formed using a gate insulating layer instead of the passivation layer.

Fig. 8 is a plan view of a thin film transistor array panel according to a second preferred embodiment of the present invention, and Fig. 9 is a cross sectional view of the thin film transistor array panel taken along the IX-IX' line
25 of Fig. 8.

A gate line assembly and a storage capacitor line assembly are formed on an insulating substrate 10 with a conductive material such as aluminum, aluminum alloy, chrome, chrome alloy, molybdenum, molybdenum alloy, chrome nitride, and molybdenum nitride while bearing a thickness of
5 1000-3500 Å.

The gate line assembly includes gate lines 22 proceeding in the horizontal direction, gate pads 24 formed at the one-sided end portions of the gate lines 22 while electrically contacting external driving circuits (not shown), and gate electrodes 26 being parts of the gate lines 22 while forming thin film
10 transistors with other components.

The storage capacitor line assembly includes rectangular-shaped storage capacitor electrode patterns 28 disposed between the neighboring gate lines 22, and storage capacitor electrode lines 29 connected to the storage capacitor electrode patterns in the neighboring pixel regions while
15 proceeding in the horizontal direction parallel to the gate lines 22.

The gate line assembly and the storage capacitor line assembly may have a multiple-layered structure where at least one layer is formed with a low resistance metallic material.

A gate insulating layer 30 with a thickness of 2500-4500 Å is formed
20 on the insulating substrate 10 with silicon nitride or silicon oxide while covering the gate line assembly and the storage capacitor line assembly.

A semiconductor pattern 42 with a thickness of 800-1500 Å is formed on the gate insulating layer 30 with amorphous silicon while being overlapped with the gate electrodes 26. Ohmic contact patterns 55 and 56

with a thickness of 500-800 Å are formed on the semiconductor pattern 42 with amorphous silicon where n type impurities are doped at high concentration.

A data line assembly and storage capacitor conductive patterns 68 are formed on the ohmic contact patterns 55 and 56 and the gate insulating layer 30 with a conductive material such as aluminum, aluminum alloy, chrome, chrome alloy, molybdenum, molybdenum alloy, chrome nitride and molybdenum nitride while bearing a thickness of 500-3500 Å.

The data line assembly includes data lines 62 proceeding in the vertical direction while crossing over the gate lines 22 to define pixel regions, data pads 64 formed at the one-sided end portions of the data lines 62 while electrically contacting external driving circuits, source electrodes 65 connected to the data lines 62 while being extended over the ohmic contact pattern 55, and drain electrodes 66 facing the source electrodes 65 while being placed over the other ohmic contact pattern 56. The drain electrodes 66 are extended over the gate insulating layer 30 within the pixel regions.

The storage capacity conductive patterns 68 are placed at the same plane as the data line assembly while bearing an island shape such that they are overlapped with the storage capacitor electrode patterns 28 while interposing the gate insulating layer 30 to thereby form storage capacitors. The storage capacitor conductive patterns 68 are electrically connected to pixel electrodes 82 to be described later to receive picture signal voltages.

The data line assembly and the storage capacitor conductive patterns 68 may have a multiple-layered structure where at least one layer is

formed with a low resistance metallic material.

A passivation layer 70 covers the data line assembly, the storage capacitor conductive patterns 68 and the semiconductor pattern 42 while bearing a thickness of 500-2000 Å. The passivation layer 70 is formed with
5 an insulating material such as silicon nitride and silicon oxide.

First and second contact holes 72 and 74 are formed at the passivation layer 70 while exposing the drain electrodes 66 and the data pads 64. Third contact holes 76 are formed at the passivation layer 70 while exposing the gate pads 24 together with the gate insulating layer 30.
10 Furthermore, fourth contact holes 78 are formed at the passivation layer 70 while exposing the storage capacitor conductive patterns 68.

Pixel electrodes 82 are formed on the passivation layer 70 such that they are electrically connected to the drain electrodes 66 and the storage capacitor conductive patterns 68 through the first and the fourth contact holes
15 72 and 78.

Subsidiary data pads 84 and subsidiary gate pads 86 are formed on the passivation layer 70 while being connected to the data pads 64 and the gate pads 24 through the second and the third contact holes 74 and 76.

The pixel electrodes 82, the subsidiary data pads 84 and the
20 subsidiary gate pads 86 are formed with a transparent conductive material such as ITO and IZO.

The pixel electrodes 82 are overlapped with the storage capacitor line assembly while interposing the passivation layer 70 and the gate insulating layer 30 to thereby form storage capacitors.

The pixel electrodes 82 are connected to the storage capacitor conductive patterns 68. In this way, the storage capacitor conductive patterns 68 form other storage capacitors in association with the storage capacitor electrode patterns 28 while interposing the gate insulating layer 30.

5 In this case, as the thickness of the gate insulating layer 30 disposed between the storage capacitor conductive patterns 68 and the storage capacitor electrode patterns 28 is small, the electrostatic capacitance of the resulting storage capacitors becomes increased even with the same overlapping area compared to the overlapping of the storage capacitor

10 electrode patterns 28 and the pixel electrodes 82. Consequently, the aperture ratio with respect to the storage capacity becomes enhanced.

A method of fabricating the thin film transistor array panel will be now explained with reference to Figs. 10A to 13B as well as Figs. 8 and 9.

As shown in Figs. 10A and 10B, a metallic layer is deposited onto an

15 insulating substrate 10, and patterned through photolithography to thereby form a gate line assembly and a storage capacitor line assembly. The gate line assembly includes gate lines 22, gate pads 24, and gate electrodes 26. The storage capacitor line assembly includes storage capacitor electrode patterns 28, and storage capacitor electrode lines 29.

20 Thereafter, as shown in Figs. 11A and 11B, a gate insulating layer 30 based on an insulating material such as silicon nitride is deposited onto the insulating substrate 10 such that it covers the gate line assembly and the storage capacitor line assembly.

An amorphous silicon layer and a conductive type impurities-doped

25 amorphous silicon layer are sequentially deposited onto the gate insulating

layer 30, and patterned through photolithography to thereby form a semiconductor pattern 42 and an ohmic contact pattern 52.

As shown in Figs. 12A and 12B, a metallic layer is deposited onto the entire surface of the substrate 10, and patterned through photolithography to
5 thereby form a data line assembly, and storage capacitor conductive patterns 68. The data line assembly includes data lines 62, data pads 64, source electrodes 65, and drain electrodes 66. The storage capacitor conductive patterns 68 are overlapped with the storage capacitor electrode patterns 28.

The ohmic contact pattern 52 is etched using the source electrode 65
10 and the drain electrode 66 as a mask to thereby separate it into a first portion 55 contacting the source electrode 65, and a second portion 56 contacting the drain electrode 66.

As shown in Figs. 13A and 13B, a passivation layer 70 is formed on the entire surface of the substrate 10 having the data line assembly, the
15 storage capacitor conductive patterns 68 and the semiconductor pattern 42 with silicon nitride or silicon oxide. The passivation layer 70 and the gate insulating layer 30 are patterned through photolithography to thereby form first to fourth contact holes 72, 74, 76 and 78. The first contact holes 72, the second contact holes 74 and the fourth contact holes 78 are formed at the
20 passivation layer 70 while exposing the drain electrodes 66, the data pads 64 and the storage capacitor conductive patterns 68, respectively. Furthermore, the third contact holes 76 are formed at the passivation layer 70 and the gate insulating layer 30 while exposing the gate pads 24.

As shown in Figs. 8 and 9, a transparent conductive layer based on
25 ITO or IZO is deposited onto the entire surface of the substrate 10.

The transparent conductive layer is patterned through photolithography to thereby form pixel electrodes 82, subsidiary data pads 84, and subsidiary gate pads 86. The pixel electrodes 82 are connected to the drain electrodes 66 and the storage capacitor conductive patterns 68 through the first and the fourth contact holes 72 and 78. The subsidiary data and gate pads 84 and 86 are connected to the data and gate pads 64 and 24 through the second and the third contact holes 74 and 76.

In this preferred embodiment, the storage capacitor conductive patterns 68 are placed at the pixel regions between the neighboring gate lines while bearing an island shape. Alternatively, the storage capacitor conductive patterns 68 may be formed at the periphery of the pixel regions while bearing a bar shape. In this case, the storage capacitor electrode patterns 28 for forming storage capacitors in association with the storage capacitor conductive patterns 68 are also formed with a bar shape.

Fig. 14 is a plan view of a thin film transistor array panel according to a third preferred embodiment of the present invention, and Fig. 15 is a cross sectional view of the thin film transistor array panel taken along the XV-XV' line of Fig. 14.

In this preferred embodiment, the storage capacitor electrode patterns 28 are placed at both peripheral sides of the pixel regions while bearing a bar shape. Of course, the respective storage capacitor electrode patterns 28 are connected to the storage capacitor electrode lines 29.

The storage capacitor conductive patterns 68 for forming storage capacitors in association with the storage capacitor electrode patterns 28 are overlapped with the storage capacitor electrode patterns 28 while interposing

the gate insulating layer 30.

The fourth contact holes 78 through which the storage capacitor conductive patterns 68 are connected to the pixel electrodes 82 are established to partially expose the storage capacitor conductive patterns 68.

5 In this structure, the storage capacitor electrode lines 29 form storage capacitors in association with the pixel electrodes 82 while interposing the gate insulating layer 30 and the passivation layer 70. Furthermore, the storage capacitor electrode patterns 28 form storage capacitors in association with the storage capacitor conductive patterns 68
10 while interposing the gate insulating layer 30.

With such a structure, the electrostatic capacitance of the resulting storage capacitors becomes increased even with the same overlapping area compared to the case where the storage capacitor electrode patterns 28 are overlapped with only the pixel electrodes 82. Consequently, the aperture
15 ratio with respect to the storage capacity becomes enhanced.

Furthermore, as the bar-shaped storage capacitor electrode patterns 28 or storage capacitor conductive patterns 68 are placed between the pixel electrodes 82 and the data lines 62, leakage of light between the pixel electrodes 82 and the data lines 62 can be prevented.

20 In the second and third preferred embodiments of the present invention, the storage capacitor line assembly is formed in a separate manner. Alternatively, parts of the gate lines may be utilized as the storage capacitor electrodes.

Fig. 16 is a plan view of a thin film transistor array panel according to
25 a fourth preferred embodiment of the present invention, and Fig. 17 is a cross

sectional view of the thin film transistor array panel taken along the XVII-XVII' line of Fig. 16.

In this preferred embodiment, the pixel electrodes arranged at any one gate line are overlapped with parts of the previous gate line to form storage capacitors. That is, parts of the gate lines are used to form the
5 desired storage capacitors without forming a storage capacitor line assembly in a separate manner.

As shown in Fig. 16, the pixel electrodes 82 at the nth gate line 22 (G_n) are overlapped with the (n-1)th gate line 22 (G_{n-1}) while being extended
10 in its area.

The storage capacitor conductive patterns 68 are partially overlapped with the gate lines 22 while interposing the gate insulating layer 30. The storage capacitor conductive patterns 68 are placed at the same plane as the data line assembly. The fourth contact holes 78 exposing the storage
15 capacitor conductive patterns 68 are formed at the passivation layer 70, and the pixel electrodes 82 at any one gate line 22 are connected to the storage capacitor conductive patterns 68 placed over the previous gate line 22 through the fourth contact holes 78.

The storage capacitor conductive patterns 68 are overlapped with the
20 gate lines 22 while interposing the gate insulating layer 30 to thereby form storage capacitors. The storage capacitor conductive patterns 68 placed over the (n-1)th gate line 22 (G_{n-1}) receive the relevant signals from the pixel electrodes 82 at the nth gate line 22 (G_n).

In the above structure, the storage capacity becomes significantly
25 increased compared to the case where the storage capacitors are formed

only through overlapping the pixel electrodes 82 with the gate lines 22. Furthermore, as a separate storage capacitor line assembly is not needed, the aperture ratio can be further enhanced.

Fig. 18 is a plan view of a thin film transistor array panel according to a fifth preferred embodiment of the present invention, and Fig. 19 is a cross sectional view of the thin film transistor array panel taken along the XIX-XIX' line of Fig. 18.

A gate line assembly and storage capacitor electrode lines 27 are formed on an insulating substrate 10 with a conductive material such as aluminum, aluminum alloy, chrome, chrome alloy, molybdenum, molybdenum alloy, chrome nitride, and molybdenum nitride while bearing a thickness of 1000-3500 Å.

The gate line assembly includes gate lines 22 proceeding in the horizontal direction, gate pads 24 formed at the one-sided end portions of the gate lines 22 while electrically contacting external driving circuits (not shown), and gate electrodes 26 being parts of the gate lines 22 while forming thin film transistors with other electrode components.

The storage capacitor electrode lines 27 are placed between the neighboring gate lines 22 while proceeding in the horizontal direction parallel to the gate lines 22.

The gate line assembly and the storage capacitor electrode lines 27 may have a multiple-layered structure where at least one layer is formed with a low resistance metallic material.

A gate insulating layer 30 with a thickness of 2500-4500 Å is formed

on the insulating substrate 10 with silicon nitride or silicon oxide while covering the gate line assembly and the storage capacitor electrode lines 27.

First contact holes 32 are formed at the gate insulating layer 30 while exposing the storage capacitor electrode lines 27.

5 A semiconductor pattern 42 with a thickness of 800-1500 Å is formed on the gate insulating layer 30 with amorphous silicon while being overlapped with the gate electrodes 26. Ohmic contact patterns 55 and 56 with a thickness of 500-800 Å are formed on the semiconductor pattern 42 with amorphous silicon where n type impurities are doped at high
10 concentration.

A data line assembly and storage capacitor conductive patterns 67 are formed on the ohmic contact patterns 55 and 56 and the gate insulating layer 30 with a conductive material such as aluminum, aluminum alloy, chrome, chrome alloy, molybdenum, molybdenum alloy, chrome nitride and
15 molybdenum nitride while bearing a thickness of 500-3500 Å.

The data line assembly includes data lines 62 proceeding in the vertical direction while crossing over the gate lines 22 to define pixel regions, data pads 64 connected to the one-sided ends of the data lines 62 while electrically contacting external driving circuits, source electrodes 65
20 protruded from the data lines 62 while being extended over the ohmic contact pattern 55, and drain electrodes 66 facing the source electrodes 65 while being placed over the other ohmic contact pattern 56. The drain electrodes 66 are extended over the gate insulating layer 30 within the pixel regions.

The storage capacity conductive patterns 67 are placed at the same

plane as the data line assembly while being connected to the storage capacitor electrode lines 27 through the first contact holes 32. The storage capacitor conductive patterns 67 are overlapped with pixel electrodes 82 to be described later to thereby form storage capacitors. The storage capacitor conductive patterns 67 are connected to the storage capacitor electrode lines 27 to receive common voltages.

The data line assembly and the storage capacitor conductive patterns 67 may have a multiple-layered structure where at least one layer is formed with a low resistance metallic material.

10 A passivation layer 70 covers the data line assembly, the storage capacitor conductive patterns 67 and the semiconductor pattern 42 while bearing a thickness of 500-2000 Å. The passivation layer 70 is formed with an insulating material such as silicon nitride and silicon oxide.

Second and third contact holes 72 and 74 are formed at the passivation layer 70 while exposing the drain electrodes 66, and the data pads 64. Fourth contact holes 76 are further formed at the passivation layer 70 while exposing the gate pads 24 together with the gate insulating layer 30.

Pixel electrodes 82 are formed on the passivation layer 70 such that they are electrically connected to the drain electrodes 66 through the second contact holes 72.

Subsidiary data pads 84 and subsidiary gate pads 86 are formed on the passivation layer 70 while being connected to the data pads 64 and the gate pads 24 through the third and the fourth contact holes 74 and 76.

The pixel electrodes 82, the subsidiary data pads 84 and the

subsidiary gate pads 86 are formed with a transparent conductive material such as ITO and IZO.

The pixel electrodes 82 are overlapped with the storage capacitor electrode lines 27 while interposing the passivation layer 70 and the gate insulating layer 30 to thereby form storage capacitors.

The pixel electrodes 82 are also overlapped with the storage capacitor conductive patterns 67 connected to the storage capacitor electrode lines 27 while interposing the passivation layer 70 to thereby form other storage capacitors. In this case, as the thickness of the passivation layer 70 disposed between the pixel electrodes 82 and the storage capacitor conductive patterns 67 is small, the electrostatic capacitance of the resulting storage capacitors becomes increased even with the same overlapping area compared to the overlapping of the storage capacitor electrode lines 27 and the pixel electrodes 82. Consequently, the aperture ratio with respect to the storage capacity becomes enhanced.

A method of fabricating the thin film transistor array panel will be now explained with reference to Figs. 20A to 24B as well as Figs. 18 and 19.

As shown in Figs. 20A and 20B, a metallic layer is deposited onto an insulating substrate 10, and patterned through photolithography to thereby form a gate line assembly and storage capacitor electrode lines 27. The gate line assembly includes gate lines 22, gate pads 24, and gate electrodes 26.

Thereafter, as shown in Figs. 21A and 21B, a gate insulating layer 30 based on an insulating material such as silicon nitride is deposited onto the insulating substrate 10 such that it covers the gate line assembly and the

storage capacitor electrode lines 27. Subsequently, an amorphous silicon layer 40 and a conductive type impurities-doped amorphous silicon layer 50 are sequentially deposited onto the gate insulating layer 30.

Thereafter, the amorphous silicon layer 40, the impurities-doped amorphous silicon layer 50 and the gate insulating layer 30 are patterned through photolithography to thereby form first contact holes 32 exposing the storage capacitor electrode lines 27.

As shown in Figs. 22A and 22B, the amorphous silicon layer 40 and the impurities-doped amorphous silicon layer 50 are patterned through photolithography to thereby form a semiconductor pattern 42 and an ohmic contact pattern 52.

As shown in Fig. 23A and 23B, a metallic layer is deposited onto the entire surface of the substrate 10, and patterned through photolithography to thereby form a data line assembly, and storage capacitor conductive patterns 67. The data line assembly includes data lines 62, data pads 64, source electrodes 65, and drain electrodes 66. The storage capacitor conductive patterns 67 are connected to the storage capacitor electrode lines 27 through the first contact holes 32.

The ohmic contact pattern 52 is etched using the source electrode 65 and the drain electrode 66 as a mask to thereby separate it into a first portion 55 contacting the source electrode 65, and a second portion 56 contacting the drain electrode 66.

As shown in Figs. 24A and 24B, a passivation layer 70 is formed on the entire surface of the substrate 10 having the data line assembly, the storage capacitor conductive patterns 67 and the semiconductor pattern 42

with silicon nitride or silicon oxide. The passivation layer 70 and the gate insulating layer 30 are patterned through photolithography to thereby form second to fourth contact holes 72, 74 and 76. The second and the third contact holes 72 and 74 are formed at the passivation layer 70 while exposing the drain electrodes 66, and the data pads 64. The fourth contact holes 76 are formed at the passivation layer 70 and the gate insulating layer 30 while exposing the gate pads 24.

As shown in Figs. 18 and 19, a transparent conductive layer based on ITO or IZO is deposited onto the entire surface of the substrate 10.

The transparent conductive layer is patterned through photolithography to thereby form pixel electrodes 82, subsidiary data pads 84, and subsidiary gate pads 86. The pixel electrodes 82 are connected to the drain electrodes 66 through the second contact holes 72. The subsidiary data and gate pads 84 and 86 are connected to the data and gate pads 64 and 24 through the third and the fourth contact holes 74 and 76.

In this preferred embodiment, the storage capacitor conductive patterns 67 are placed at the pixel regions between the neighboring gate lines. Alternatively, the storage capacitor conductive patterns 67 may be formed at the periphery of the pixel regions while bearing a bar shape.

Fig. 25 is a plan view of a thin film transistor array panel according to a sixth preferred embodiment of the present invention, and Fig. 26 is a cross sectional view of the thin film transistor array panel taken along the XXVI-XXVI' line of Fig. 25.

In this preferred embodiment, the storage capacitor conductive patterns 67 are placed at both peripheral sides of the pixel regions while

bearing a bar shape. The storage capacitor conductive patterns 67 are connected to the storage capacitor electrode lines 27 through the first contact holes 32 formed at the gate insulating layer 30.

The storage capacitor electrode lines 27 form storage capacitors in association with the pixel electrodes 82 while interposing the gate insulating layer 30 and the passivation layer 70. Furthermore, the storage capacitor conductive patterns 67 form other storage capacitors in association with the pixel electrodes 82 while interposing the passivation layer 70.

With such a structure, the electrostatic capacitance of the storage capacitors becomes increased even with the same overlapping area compared to the case where only the storage capacitor electrode lines 27 are overlapped with the pixel electrodes 82. Consequently, the aperture ratio with respect to the storage capacity becomes enhanced.

Furthermore, as the bar-shaped storage capacitor conductive patterns 67 are placed between the pixel electrodes 82 and the data lines 62, leakage of light between the pixel electrodes 82 and the data lines 62 can be prevented.

In the fifth and sixth preferred embodiments of the present invention, the storage capacitor line assembly is formed in a separate manner. Alternatively, parts of the gate lines may be utilized as the storage capacitor electrodes.

Fig. 27 is a plan view of a thin film transistor array panel according to a seventh preferred embodiment of the present invention, and Fig. 28 is a cross sectional view of the thin film transistor array panel taken along the XXVIII-XXVIII' line of Fig. 27.

In this preferred embodiment, the pixel electrodes arranged at any one gate line are overlapped with parts of the previous gate line to form storage capacitors. That is, parts of the gate lines are used to form the desired storage capacitors without forming a storage capacitor line assembly
5 in a separate manner.

As shown in Fig. 27, the pixel electrodes 82 at the n th gate line 22 (G_n) are overlapped with the $(n-1)$ th gate line 22 (G_{n-1}) while being extended in its area.

The storage capacitor conductive patterns 67 are partially overlapped
10 with the gate lines 22 while interposing the gate insulating layer 30. The storage capacitor conductive patterns 67 are placed at the same plane as the data line assembly. The fourth contact holes 78 exposing the storage capacitor conductive patterns 67 are formed at the passivation layer 70. The storage capacitor conductive patterns 67 placed over the $(n-1)$ th gate
15 line 22 (G_{n-1}) are connected to the pixel electrodes 82 at the n th gate line 22 (G_n).

The storage capacitor conductive patterns 67 are overlapped with the gate lines 22 while interposing the gate insulating layer 30 to thereby form storage capacitors. The storage capacitor conductive patterns 68 placed
20 over the $(n-1)$ th gate line 22 (G_{n-1}) receive the relevant signals from the pixel electrodes 82 at the n th gate line 22 (G_n).

In the above structure, the storage capacity becomes significantly increased compared to the case where the storage capacitors are formed only through overlapping the pixel electrodes 82 with the gate lines 22.
25 Furthermore, as a separate storage capacitor line assembly is not needed,

the aperture ratio can be further enhanced.

The inventive structure may be well adapted for use with all of the liquid crystal display modes. Particularly, in case such a structure is employed for use with the optically compensated birefringence (OCB) mode, various advantages are resulted.

As the $\Delta \epsilon$ value of the liquid crystal is great with the OCB mode liquid crystal display, the difference between the dielectric constant at the initial state and the dielectric constant at the succeeding state as a function of the gray values is also great, and therefore, variation in the liquid crystal voltage is inevitably made to a large scale.

Meanwhile, as shown in Fig. 29, the waveform (time-brightness) curve of the response speed measured with all of the liquid crystal display modes bears a two-stepped waveform exhibiting two stepped differences.

As the response speed is measured while altering the total brightness from 10% to 90%, it turns out to be slower in case the brightness at the two-stepped portion is less than 90%.

The OCB mode liquid crystal display exhibits a characteristic in that the two-stepped waveform occurs at the first frame, and a normal brightness is maintained at the second frame or the third frame. Therefore, in case the electrostatic capacitance at the two-stepped portion is increased to be 90% or more, particularly 95% or more, the desired normal brightness can be maintained at the first frame, thereby making rapid response speed.

Table 1 lists the brightness values at the two-stepped portion over the waveform (time-brightness) curve of the response speed as a function of

the ratio of the electrostatic capacitance C_{st} of the storage capacitors to the electrostatic capacitance C_{lc} of the liquid crystal in the OCB mode liquid crystal display.

Table 1

Clc:Cst	1.00:0.70	1.00:0.91
Two-stepped portion (brightness%)	81.8%	87.3%

5

It can be known from Table 1 that as the storage capacity C_{st} is increased, the brightness at the two-stepped portion is approximated to 90%. Therefore, the rapid response speed can be obtained through increasing the storage capacity such that the brightness at the two-stepped portion goes over 90%. Particularly, in case the storage capacity is increased such that the brightness at the two-stepped portion goes over 95%, the response speed can be further enhanced. In order to increase the storage capacity to such a degree, the storage capacitors according to the first to seventh preferred embodiments may be applied for use in the OCB mode liquid crystal display. That is, the storage capacitor electrode lines are formed at the same plane as the data line assembly such that they are overlapped with the pixel electrodes while interposing only the passivation layer. In this structure, the storage capacity as well as the aperture ratio are significantly enhanced without enlarging the area of the storage capacitor electrode lines, compared to the case where the storage capacitor electrode lines are formed at the same plane as the gate line assembly such that they are overlapped

15
20

with the pixel electrodes while interposing the passivation layer and the gate insulating layer. As only one of the passivation layer and the gate insulating layer is disposed between the storage capacitor electrodes, it is not needed to enlarge the area of the storage capacitor electrode components.

5 Consequently, the storage capacity can be increased without decreasing the aperture ratio.

As described above, with the inventive structure, the storage capacity can be increased without decreasing the aperture ratio while enhancing the response speed.

10 While the present invention has been described in detail with reference to the preferred embodiments, those skilled in the art will appreciate that various modifications and substitutions can be made thereto without departing from the spirit and scope of the present invention as set forth in the appended claims.

WHAT IS CLAIMED IS:

1. A thin film transistor array panel comprising:
 - an insulating substrate;
 - a gate line assembly formed on the insulating substrate with gate
 - 5 lines, and gate electrodes;
 - a gate insulating layer covering the gate line assembly;
 - a semiconductor pattern formed on the gate insulating layer;
 - a data line assembly formed on the gate insulating layer overlaid with
 - the semiconductor pattern, the data line assembly having data lines crossing
 - 10 over the gate lines, source electrodes connected to the data lines, and drain
 - electrodes facing the source electrodes;
 - storage capacitor electrode lines formed between the neighboring
 - data lines while crossing over the gate lines;
 - a passivation layer covering the data line assembly, the storage
 - 15 capacitor electrode lines and the semiconductor pattern while bearing contact
 - holes exposing the drain electrodes; and
 - pixel electrodes formed on the passivation layer while being
 - connected to the drain electrodes through the contact holes, the pixel
 - electrodes being overlapped with the storage capacitor electrode lines.
- 20 2. The thin film transistor array panel of claim 1 further comprising a common interconnection line commonly interconnecting the storage capacitor electrode lines.
3. The thin film transistor array panel of claim 2 wherein the common interconnection line is formed with the same material as the pixel
- 25 electrodes while crossing over the data lines in an insulated manner.

4. The thin film transistor array panel of claim 2 wherein the common interconnection line is formed with the same material as the gate lines while crossing over the data lines in an insulated manner.

5. The thin film transistor array panel of claim 3 wherein the passivation layer has a plurality of contact holes exposing the storage capacitor electrode lines, and the common interconnection line is connected to the storage capacitor electrode lines through the contact holes.

6. The thin film transistor array panel of claim 2 further comprising a subsidiary interconnection line connected to the storage capacitor electrode lines.

7. The thin film transistor array panel of claim 6 wherein the storage capacitor electrode lines and the subsidiary interconnection line are formed with the same material.

8. The thin film transistor array panel of claim 1 further comprising:

gate pads formed at one-sided end portions of the gate lines;

data pads formed at one-sided end portions of the data lines;

first contact holes formed at the passivation layer and the gate insulating layer while exposing the gate pads;

20 second contact holes formed at the passivation layer while exposing the data pads; and

subsidiary gate and data pads connected to the gate and the data pads through the first and the second contact holes.

9. A liquid crystal display comprising:

25 the thin film transistor array panel of claim 1;

a counter substrate facing the thin film transistor array panel; and
a liquid crystal layer sandwiched between the thin film transistor array panel and the counter panel.

10. The liquid crystal display of claim 9 having storage capacitors
5 with an electrostatic capacitance greater than the electrostatic capacitance of the liquid crystal layer by 90% or more.

11. The liquid crystal display of claim 10 wherein the electrostatic capacitance of the storage capacitors is greater than the electrostatic capacitance of the liquid crystal layer by 95% or more.

10 12. The liquid crystal display of claim 9 wherein the thin film transistor array panel further comprises a common interconnection line commonly interconnecting the storage capacitor electrode lines.

13. The liquid crystal display of claim 12 wherein the common interconnection line is formed with the same material as the pixel electrodes
15 while crossing over the data lines in an insulated manner.

14. The liquid crystal display of claim 13 wherein the passivation layer has a plurality of contact holes exposing the storage capacitor electrode lines, and the common interconnection line is connected to the storage capacitor electrode lines through the contact holes.

20 15. The liquid crystal display of claim 12 wherein the thin film transistor array panel further comprises a subsidiary interconnection line connected to the storage capacitor electrode lines.

16. The liquid crystal display of claim 15 wherein the storage capacitor electrode lines and the subsidiary interconnection line are formed
25 with the same material.

17. A thin film transistor array panel comprising:

an insulating substrate;

a gate line assembly and a storage capacitor line assembly formed
on the insulating substrate, the gate line assembly having gate lines and gate
5 electrodes;

a gate insulating layer covering the gate line assembly and the
storage capacitor line assembly;

a semiconductor pattern formed on the gate insulating layer;

a data line assembly and storage capacitor conductive patterns
10 formed on the gate insulating layer overlaid with the semiconductor pattern,
the data line assembly having data lines, source electrodes and drain
electrodes, the storage capacitor conductive patterns being partially
overlapped with the storage capacitor line assembly to thereby form first
storage capacitors;

15 a passivation layer covering the data line assembly, the storage
capacitor conductive patterns and the semiconductor pattern;

first and second contact holes formed at the passivation layer while
exposing the drain electrodes and the storage capacitor conductive patterns,
respectively; and

20 pixel electrodes formed on the passivation layer while being
connected to the drain electrodes and the storage capacitor conductive
patterns through the first and the second contact holes, the pixel electrodes
forming second storage capacitors in association with parts of the storage
capacitor line assembly.

25 18. The thin film transistor array panel of claim 17 wherein the

storage capacitor line assembly has storage capacitor electrode lines proceeding parallel to the gate lines, and storage capacitor electrode patterns connected to the storage capacitor electrode lines.

19. The thin film transistor array panel of claim 18 wherein the
5 storage capacitor electrode patterns are overlapped with the storage capacitor conductive patterns to thereby form the first storage capacitors, and the storage capacitor electrode lines are overlapped with the pixel electrodes to thereby form the second storage capacitors.

20. The thin film transistor array panel of claim 19 wherein the
10 storage capacitor electrode patterns are formed within pixel regions defined by the gate lines and the data lines.

21. The thin film transistor array panel of claim 19 wherein the
storage capacitor electrode patterns are formed with a bar shape along the data lines while being overlapped with peripheral portions of the pixel
15 electrodes.

22. A liquid crystal display comprising:
the thin film transistor array panel of claim 17;
a counter substrate facing the thin film transistor array panel; and
a liquid crystal layer sandwiched between the thin film transistor
20 array panel and the counter panel.

23. The liquid crystal display of claim 22 wherein the first and the second storage capacitors have an electrostatic capacitance greater than the electrostatic capacitance of the liquid crystal layer by 90% or more.

24. A thin film transistor array panel comprising:
25 an insulating substrate;

a gate line assembly formed on the insulating substrate, the gate line assembly having first gate lines, gate electrodes connected to the first gate lines, and second gate lines spaced apart from the first gate lines with a predetermined distance;

5 a gate insulating layer covering the gate line assembly;

a semiconductor pattern formed on the gate insulating layer while being overlapped with the gate electrodes;

a data line assembly and storage capacitor conductive patterns formed on the gate insulating layer overlaid with the semiconductor pattern,
10 the data line assembly having data lines crossing over the first and the second gate lines, source electrodes and drain electrodes, the storage capacitor conductive patterns being partially overlapped with the second gate lines to thereby form first storage capacitors;

a passivation layer covering the data line assembly, the storage
15 capacitor conductive patterns and the semiconductor pattern;

first and second contact holes formed at the passivation layer while exposing the drain electrodes and the storage capacitor conductive patterns, respectively; and

pixel electrodes formed at the passivation layer while being
20 connected to the drain electrodes and the storage capacitor conductive patterns through the first and the second contact holes, the pixel electrodes being partially overlapped with the second gate lines to thereby form second storage capacitors.

25. A liquid crystal display comprising:

25 the thin film transistor array panel of claim 24;

a counter substrate facing the thin film transistor array panel; and
a liquid crystal layer sandwiched between the thin film transistor array panel and the counter panel.

26. The liquid crystal display of claim 25 wherein the first and the
5 second storage capacitors have an electrostatic capacitance greater than the electrostatic capacitance of the liquid crystal layer by 90% or more.

27. A thin film transistor array panel comprising:
an insulating substrate;
a gate line assembly and storage capacitor electrode lines formed on
10 the insulating substrate, the gate line assembly having gate lines and gate electrodes;

a gate insulating layer covering the gate line assembly and the storage capacitor electrode lines;

first contact holes formed at the gate insulating layer while exposing
15 the storage capacitor electrode lines;

a semiconductor pattern formed on the gate insulating layer while being overlapped with the gate electrodes;

a data line assembly and storage capacitor conductive patterns formed on the gate insulating layer overlaid with the semiconductor pattern,
20 the data line assembly having data lines, source electrodes and drain electrodes, the storage capacitor conductive patterns being connected to the storage capacitor electrode lines through the first contact holes;

a passivation layer covering the data line assembly, the storage capacitor conductive patterns and the semiconductor pattern;

25 second contact holes formed at the passivation layer while exposing

the drain electrodes; and

pixel electrodes formed at the passivation layer while being connected to the drain electrodes through the second contact holes, the pixel electrodes being overlapped with the storage capacitor conductive patterns to thereby form first storage capacitors while being partially overlapped with the storage capacitor electrode lines to thereby form second storage capacitors.

28. The thin film transistor array panel of claim 27 wherein the storage capacitor electrode lines proceed parallel to the gate lines.

10 29. The thin film transistor array panel of claim 27 wherein the storage capacitor conductive patterns are overlapped with the storage capacitor electrode lines.

30. The thin film transistor array panel of claim 29 wherein the storage capacitor conductive patterns are formed within pixel regions defined by the gate lines and the data lines.

31. The thin film transistor array panel of claim 27 wherein the storage capacitor electrode patterns are formed with a bar shape along the data lines while being overlapped with peripheral portions of the pixel electrodes.

20 32. A liquid crystal display comprising:
the thin film transistor array panel of claim 27;
a counter substrate facing the thin film transistor array panel; and
a liquid crystal layer sandwiched between the thin film transistor array panel and the counter panel.

25 33. The liquid crystal display of claim 32 wherein the first and the

second storage capacitors have an electrostatic capacitance greater than the electrostatic capacitance of the liquid crystal layer by 90% or more.

34. A thin film transistor array panel comprising:

an insulating substrate;

5 a gate line assembly formed on the insulating substrate, the gate line assembly having first gate lines, gate electrodes connected to the first gate lines, and second gate lines spaced apart from the first gate lines with a predetermined distance;

a gate insulating layer covering the gate line assembly;

10 first contact holes formed at the gate insulating layer while partially exposing the second gate lines;

a semiconductor pattern formed on the gate insulating layer while being overlapped with the gate electrodes;

a data line assembly and storage capacitor conductive patterns
15 formed on the gate insulating layer overlaid with the semiconductor pattern, the data line assembly having data lines crossing over the first and the second gate lines, source electrodes and drain electrodes, the storage capacitor conductive patterns being connected to the second gate lines through the first contact holes;

20 a passivation layer covering the data line assembly, the storage capacitor conductive patterns and the semiconductor pattern;

second contact holes formed at the passivation layer while exposing the drain electrodes; and

pixel electrodes formed at the passivation layer while being
25 connected to the drain electrodes through the second contact holes, the pixel

electrodes being overlapped with the storage capacitor conductive patterns to thereby form first storage capacitors while being partially overlapped with the second gate lines to thereby form second storage capacitors.

35. A liquid crystal display comprising:

5 the thin film transistor array panel of claim 34;

a counter substrate facing the thin film transistor array panel; and

a liquid crystal layer sandwiched between the thin film transistor array panel and the counter panel.

36. The liquid crystal display of claim 35 wherein the first and the
10 second storage capacitors have an electrostatic capacitance greater than the electrostatic capacitance of the liquid crystal layer by 90% or more.

37. A method of fabricating a thin film transistor array panel, the method comprising the steps of:

forming a gate line assembly and a storage capacitor line assembly
15 on an insulating substrate such that the gate line assembly has gate lines and gate electrodes;

forming a gate insulating layer such that the gate insulating layer covers the gate line assembly and the storage capacitor line assembly;

forming a semiconductor pattern on the gate insulating layer;

20 forming a data line assembly and storage capacitor conductive patterns on the gate insulating layer overlaid with the semiconductor pattern such that the data line assembly has data lines, source electrodes and drain electrodes, and the storage capacitor conductive patterns are partially overlapped with the storage capacitor line assembly to thereby form first
25 storage capacitors;

forming a passivation layer such that the passivation layer covers the data line assembly, the storage capacitor conductive patterns and the semiconductor pattern;

forming first and second contact holes at the passivation layer such
5 that the first and the second contact holes expose the drain electrodes and the storage capacitor conductive patterns, respectively; and

forming pixel electrodes on the passivation layer such that the pixel electrodes are connected to the drain electrodes and the storage capacitor conductive patterns through the first and the second contact holes while
10 forming second storage capacitors in association with parts of the storage capacitor lines assembly.

38. The method of claim 37 wherein the storage capacitor line assembly has storage capacitor electrode lines proceeding parallel to the gate lines, and storage capacitor electrode patterns connected to the storage
15 capacitor electrode lines.

39. A method of fabricating a thin film transistor array panel, the method comprising the steps of:

forming a gate line assembly on an insulating substrate such that the gate line assembly has first gate lines, gate electrodes connected to the first
20 gate lines, and second gate lines spaced apart from the first gate lines with a predetermined distance while proceeding parallel to the first gate lines;

forming a gate insulating layer such that the gate insulating layer covers the gate line assembly;

forming a semiconductor pattern on the gate insulating layer such
25 that the semiconductor pattern is overlapped with the gate electrodes;

forming a data line assembly and storage capacitor conductive patterns on the gate insulating layer overlaid with the semiconductor pattern such that the data line assembly has data lines crossing over the first and the second gate lines, source electrodes and drain electrodes, and the storage capacitor conductive patterns are partially overlapped with the second gate lines to thereby form first storage capacitors;

forming a passivation layer such that the passivation layer covers the data line assembly, the storage capacitor conductive patterns and the semiconductor pattern;

10 forming first and second contact holes at the passivation layer such that the first and the second contact holes expose the drain electrodes and the storage capacitor conductive patterns, respectively; and

forming pixel electrodes on the passivation layer such that the pixel electrodes are connected to the drain electrodes and the storage capacitor conductive patterns through the first and the second contact holes while forming second storage capacitors in association with parts of the second gate lines.

40. A method of fabricating a thin film transistor array panel, the method comprising the steps of:

20 forming a gate line assembly and storage capacitor electrode lines on an insulating substrate such that the gate line assembly has gate lines and gate electrodes;

forming a gate insulating layer such that the gate insulating layer covers the gate line assembly and the storage capacitor electrode lines;

25 forming first contact holes at the gate insulating layer such that the

first contact holes expose the storage capacitor electrode lines;

forming a semiconductor pattern on the gate insulating layer such that the semiconductor pattern is overlapped with the gate electrodes;

forming a data line assembly and storage capacitor conductive
5 patterns on the gate insulating layer overlaid with the semiconductor pattern such that the data line assembly has data lines, source electrodes and drain electrodes, and the storage capacitor conductive patterns are connected to the storage capacitor electrode lines through the first contact holes;

forming a passivation layer such that the passivation layer covers the
10 data line assembly, the storage capacitor conductive patterns and the semiconductor pattern;

forming second contact holes at the passivation layer such that the second contact holes expose the drain electrodes; and

forming pixel electrodes on the passivation layer such that the pixel
15 electrodes are connected to the drain electrodes through the second contact holes, the pixel electrodes being overlapped with the storage capacitor conductive patterns to thereby form first storage capacitors while being partially overlapped with the storage capacitor electrode lines to thereby form second storage capacitors.

20 41. A method of fabricating a thin film transistor array panel, the method comprising the steps of:

forming a gate line assembly on an insulating substrate such that the gate line assembly has first gate lines, gate electrodes connected to the first gate lines, and second gate lines spaced apart from the first gate lines with a
25 predetermined distance while proceeding parallel to the first gate lines;

forming a gate insulating layer such that the gate insulating layer covers the gate line assembly;

forming first contact holes at the gate insulating layer such that the first contact holes partially expose the second gate lines;

5 forming a semiconductor pattern on the gate insulating layer such that the semiconductor pattern is overlapped with the gate electrodes;

forming a data line assembly and storage capacitor conductive patterns on the gate insulating layer overlaid with the semiconductor pattern such that the data line assembly has data lines crossing over the first and the
10 second gate lines, source electrodes and drain electrodes, and the storage capacitor conductive patterns are connected to the second gate lines through the first contact holes;

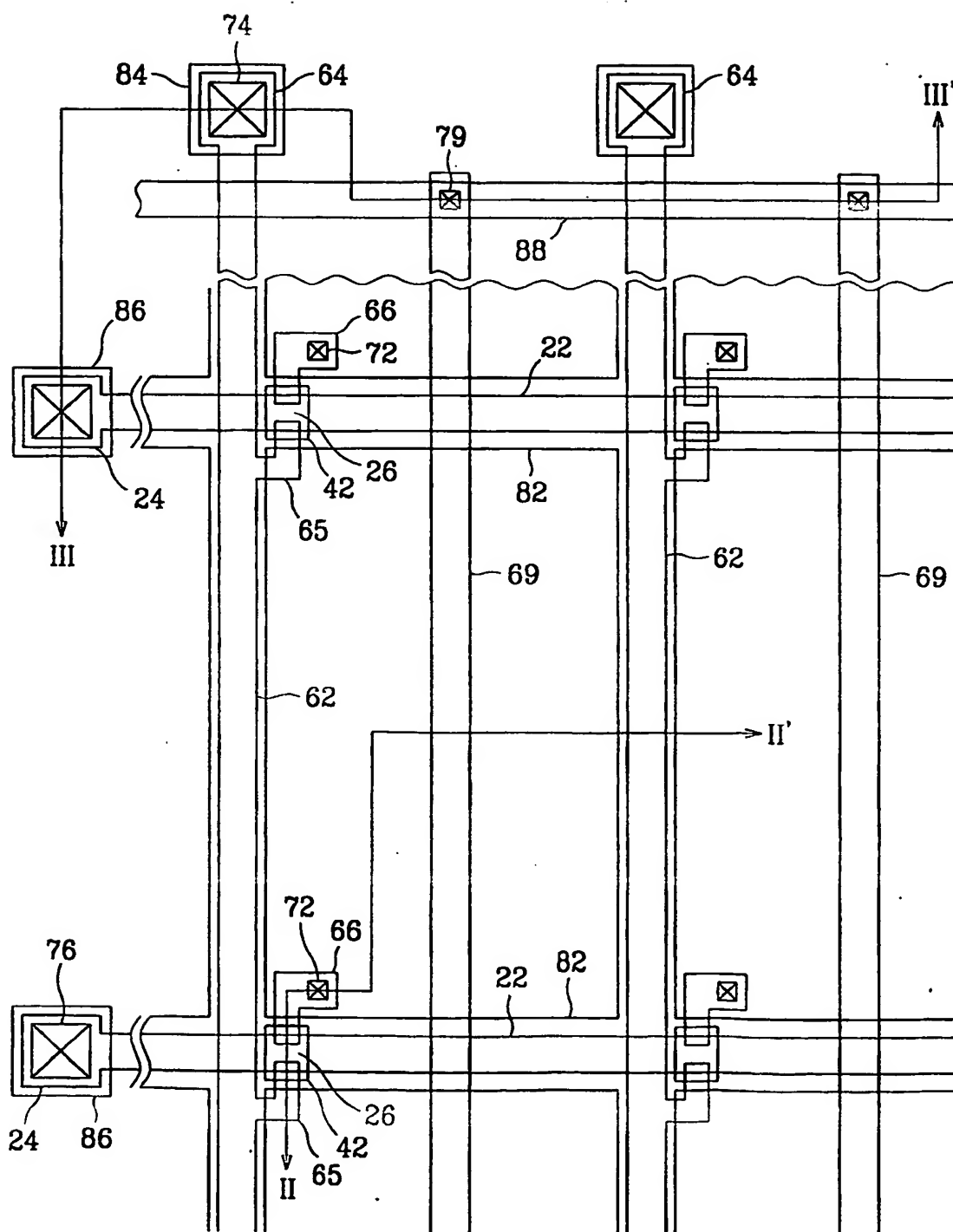
forming a passivation layer such that the passivation layer covers the data line assembly, the storage capacitor conductive patterns and the
15 semiconductor pattern;

forming second contact holes at the passivation layer such that the second contact holes expose the drain electrodes; and

forming pixel electrodes on the passivation layer such that the pixel electrodes are connected to the drain electrodes through the second contact
20 holes, the pixel electrodes being overlapped with the storage capacitor conductive patterns to thereby form first storage capacitors while being partially overlapped with the second gate lines to thereby form second storage capacitors.

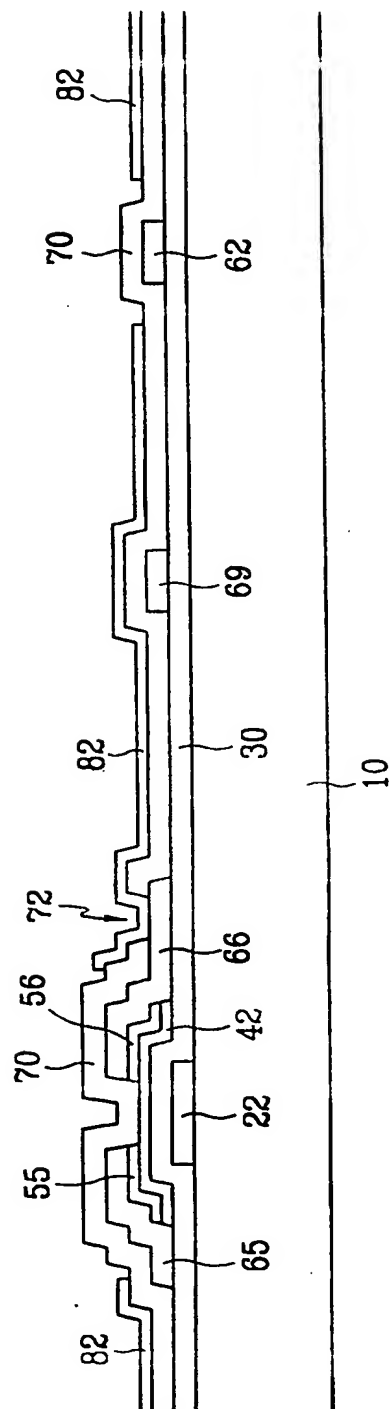
1/44

FIG.1



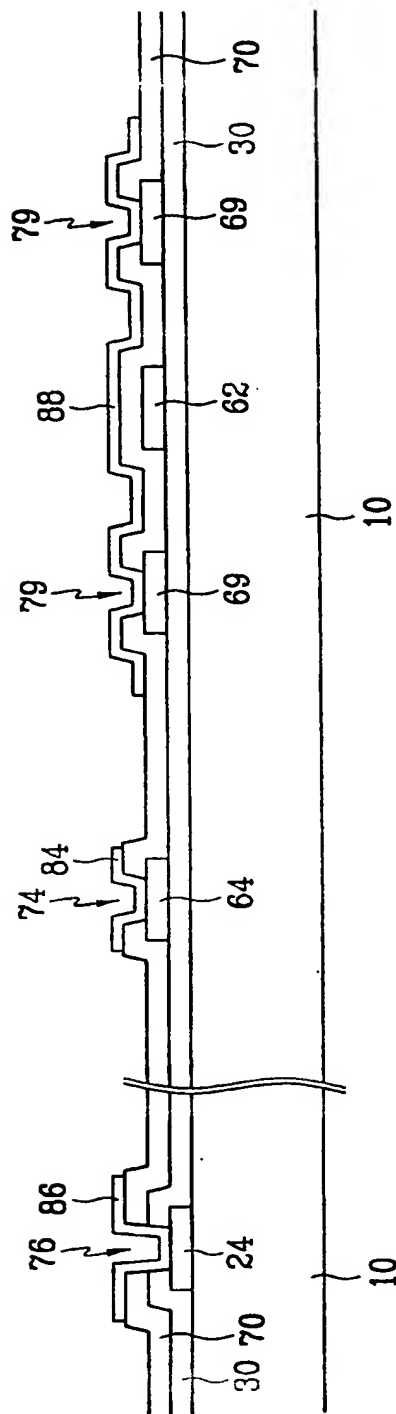
2/44

FIG.2



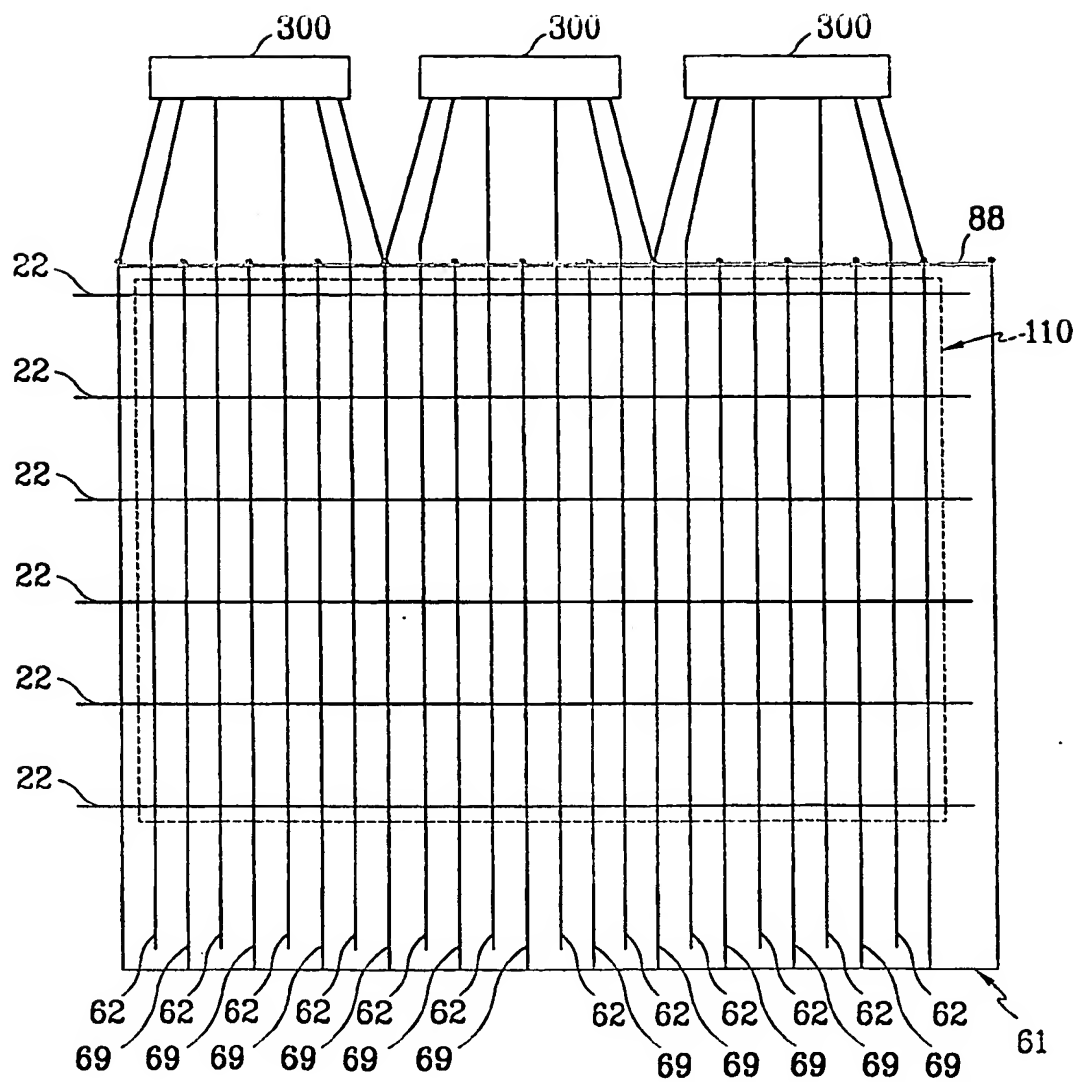
3/44

FIG. 3



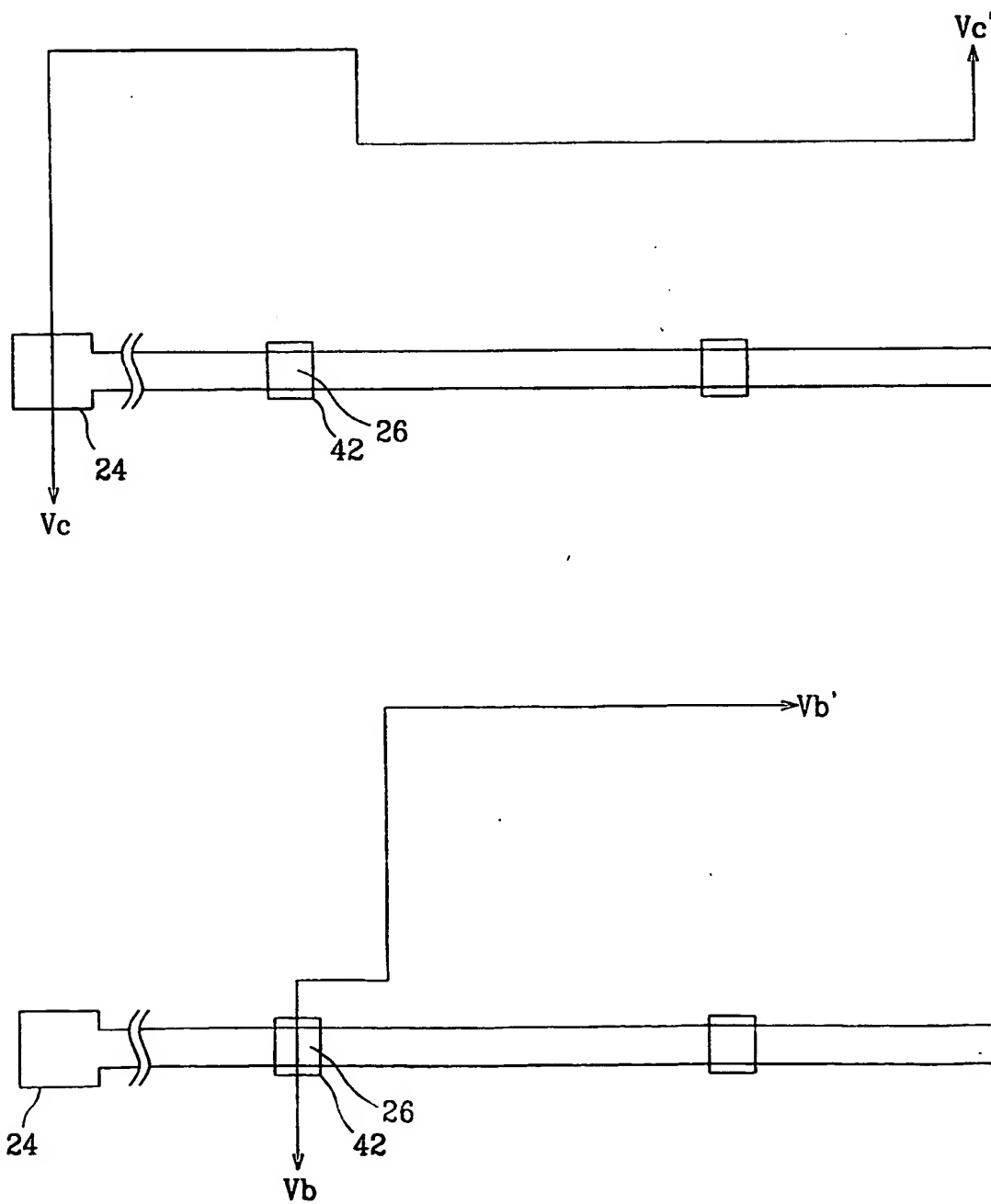
4/44

FIG. 4



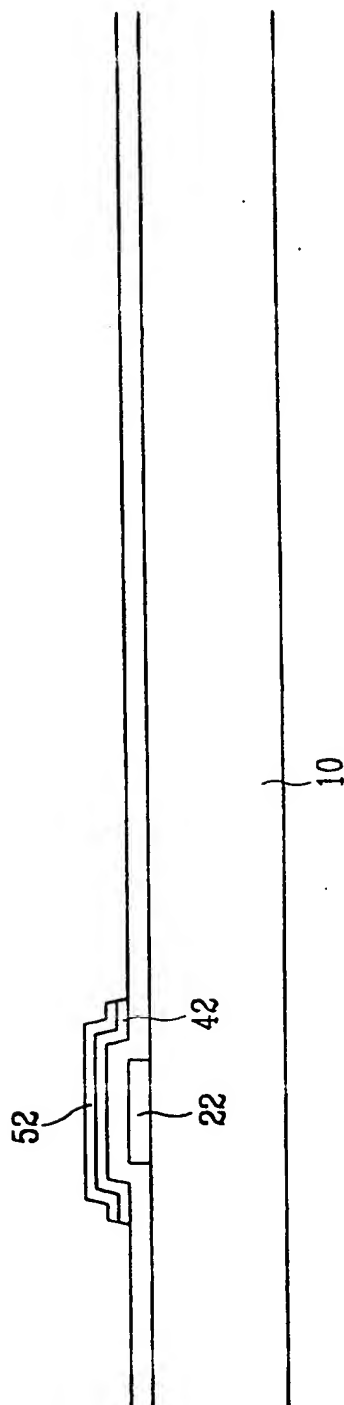
5/44

FIG.5a



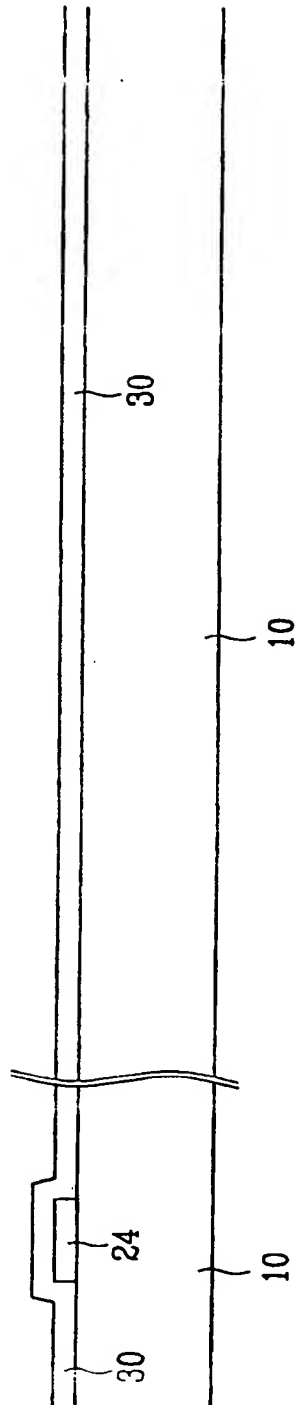
6/44

FIG. 5b



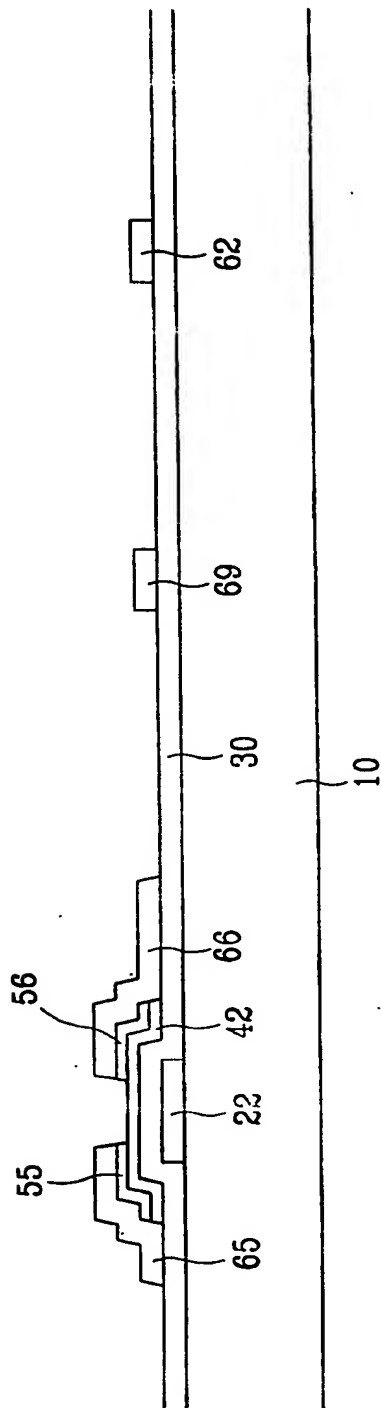
7/44

FIG. 5c



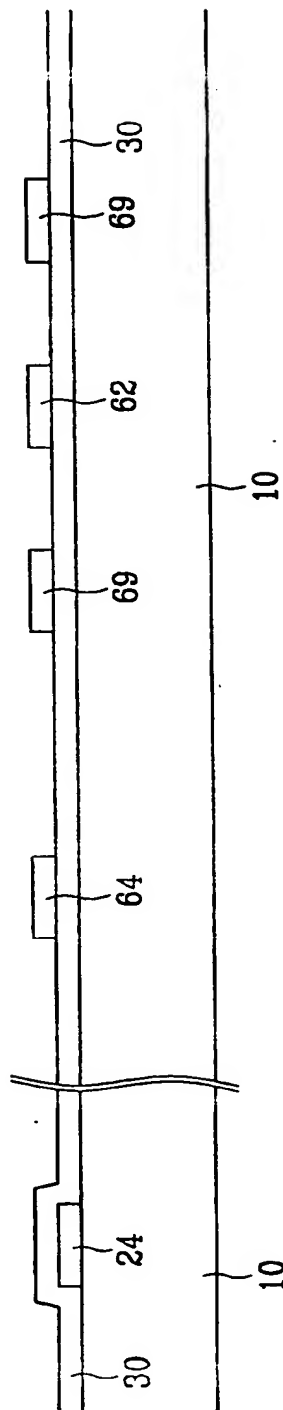
9/44

FIG. 6b



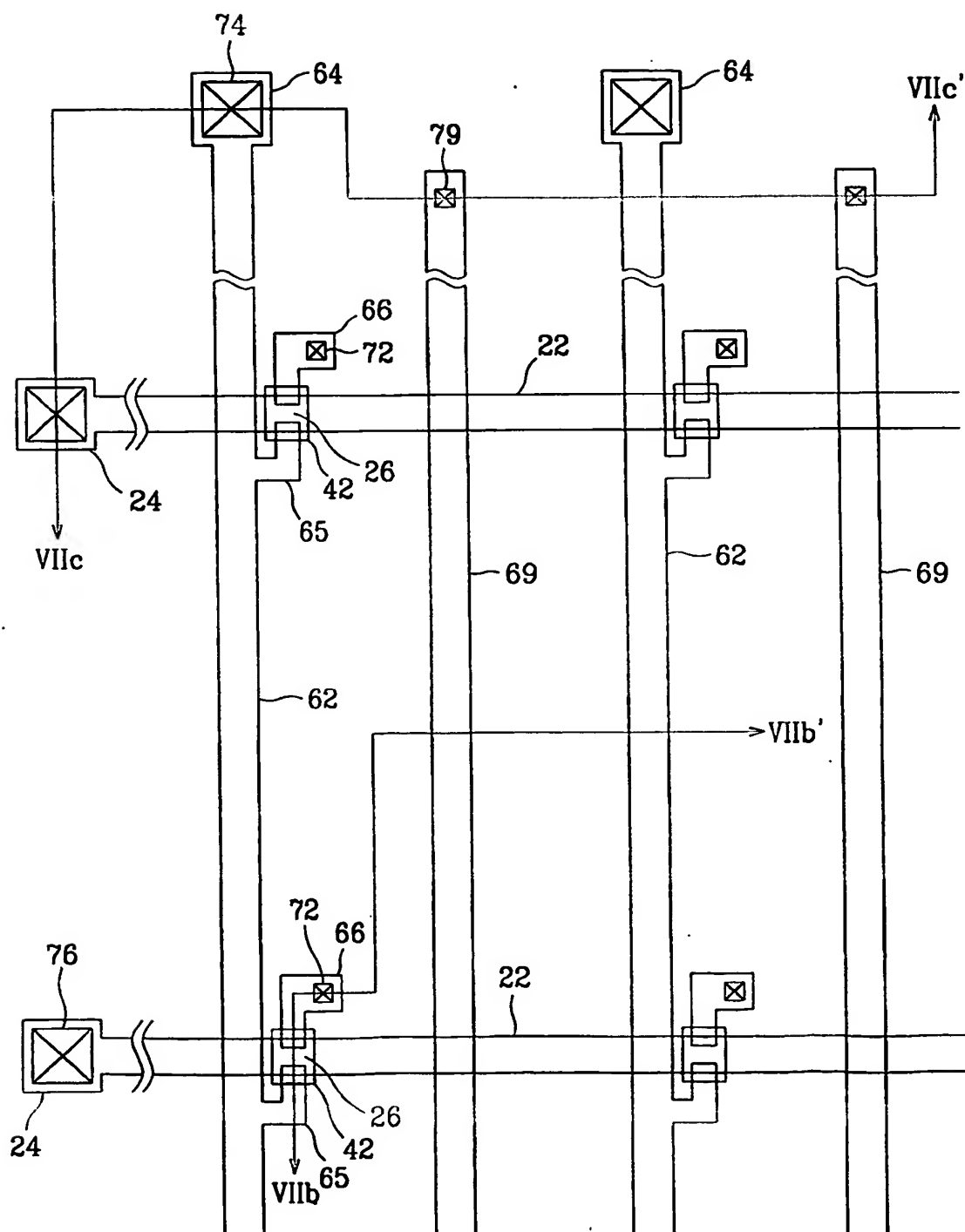
10/44

FIG. 6c



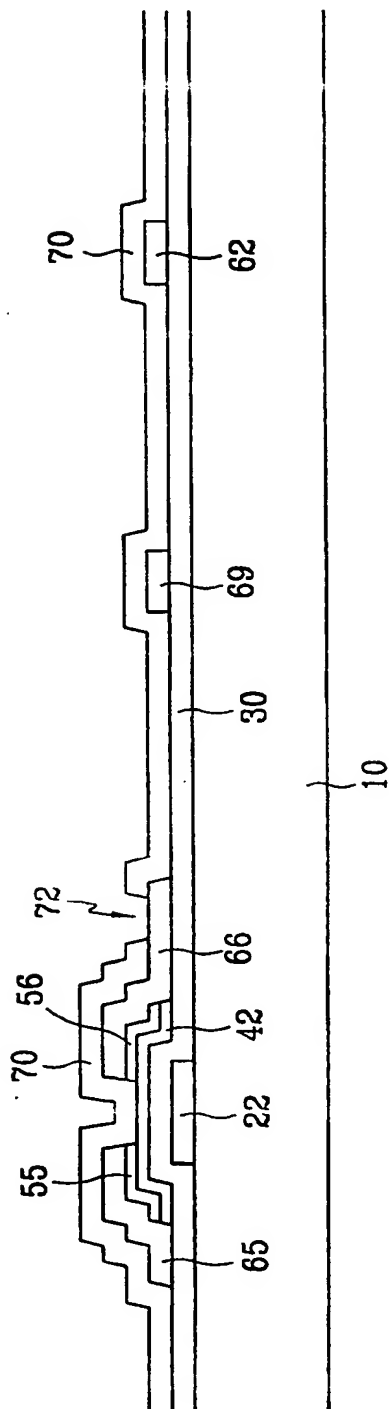
11/44

FIG. 7a



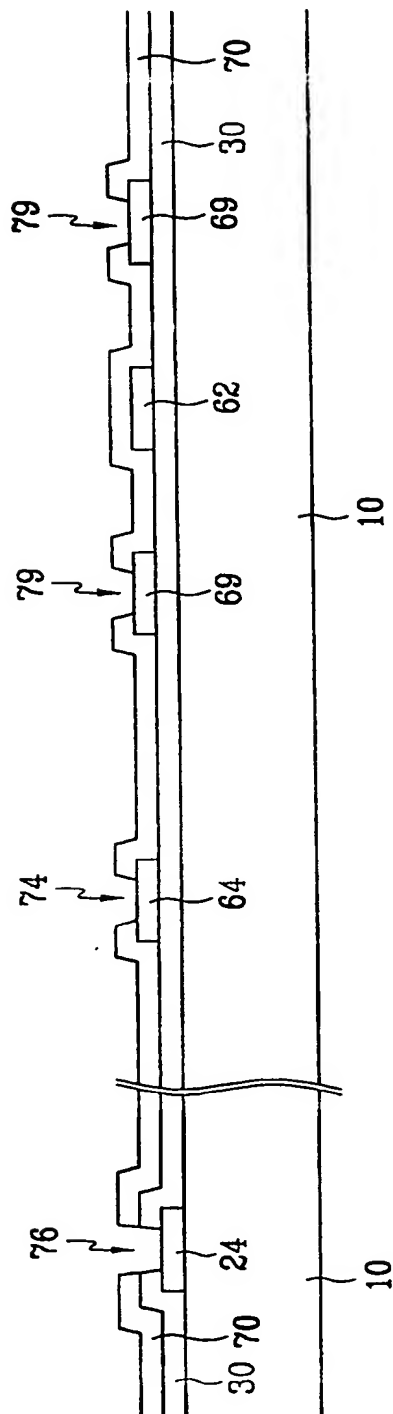
12/44

FIG. 7b



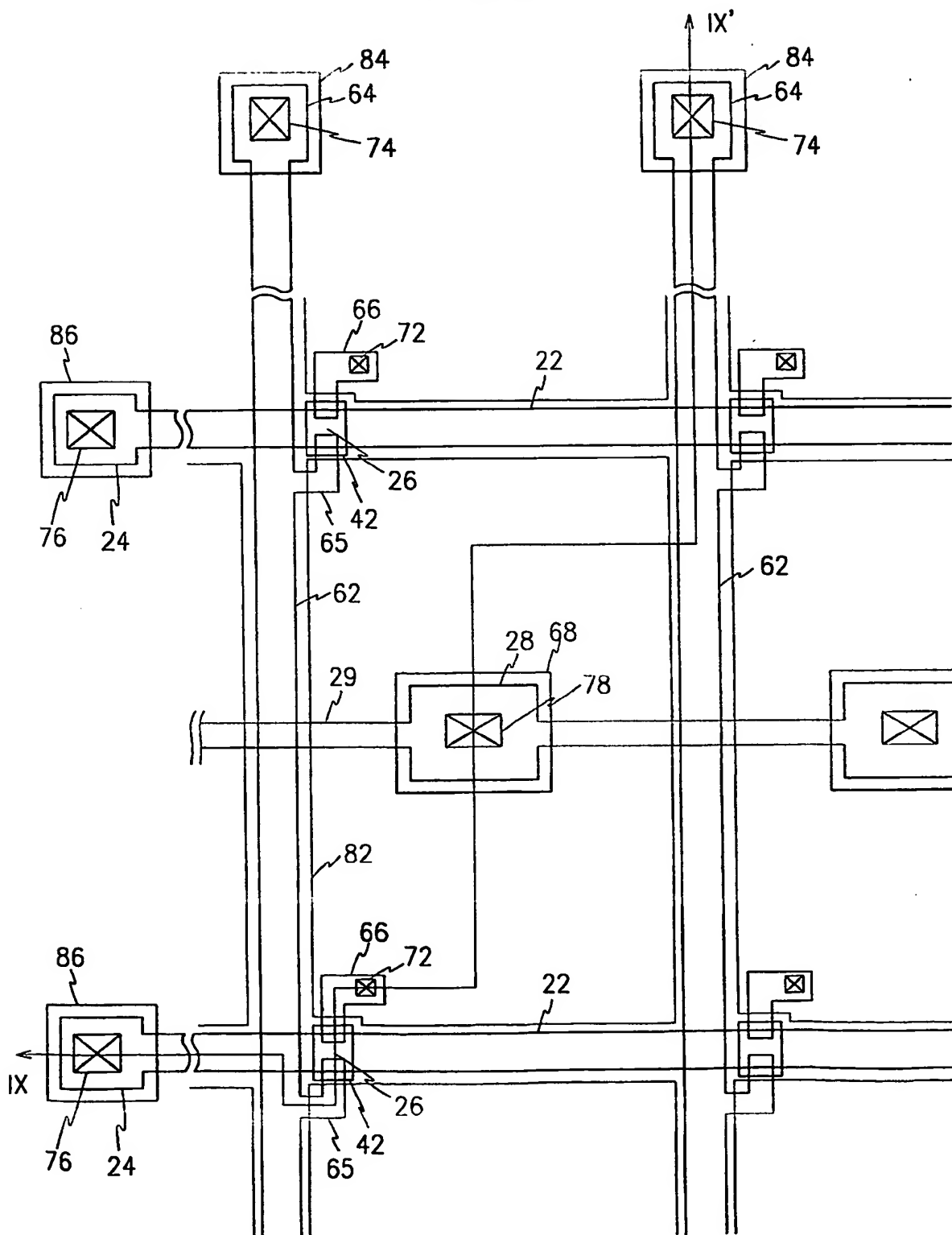
13/44

FIG. 7C



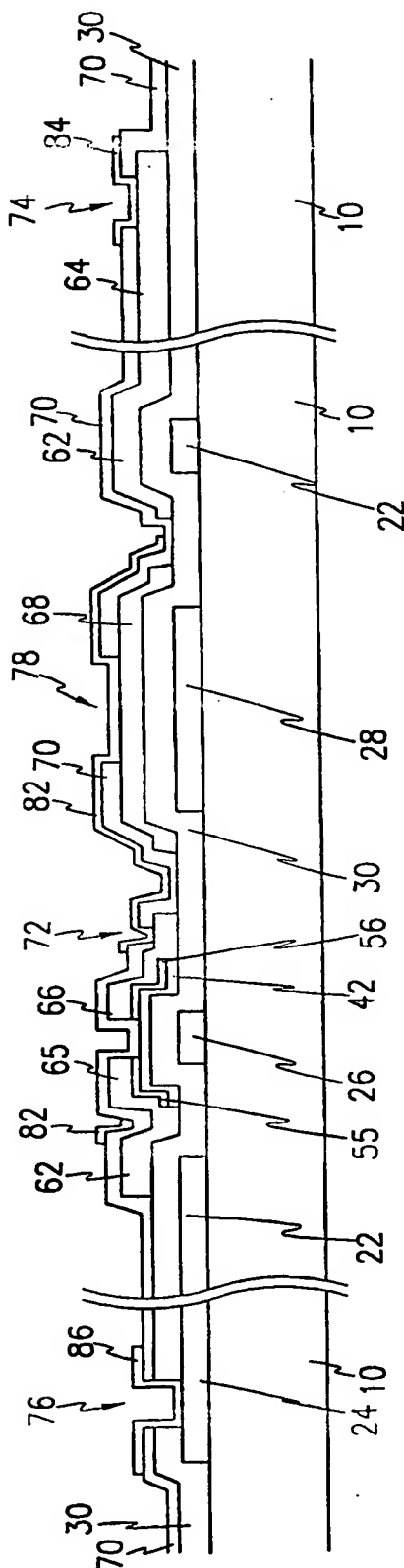
14/44

FIG. 8



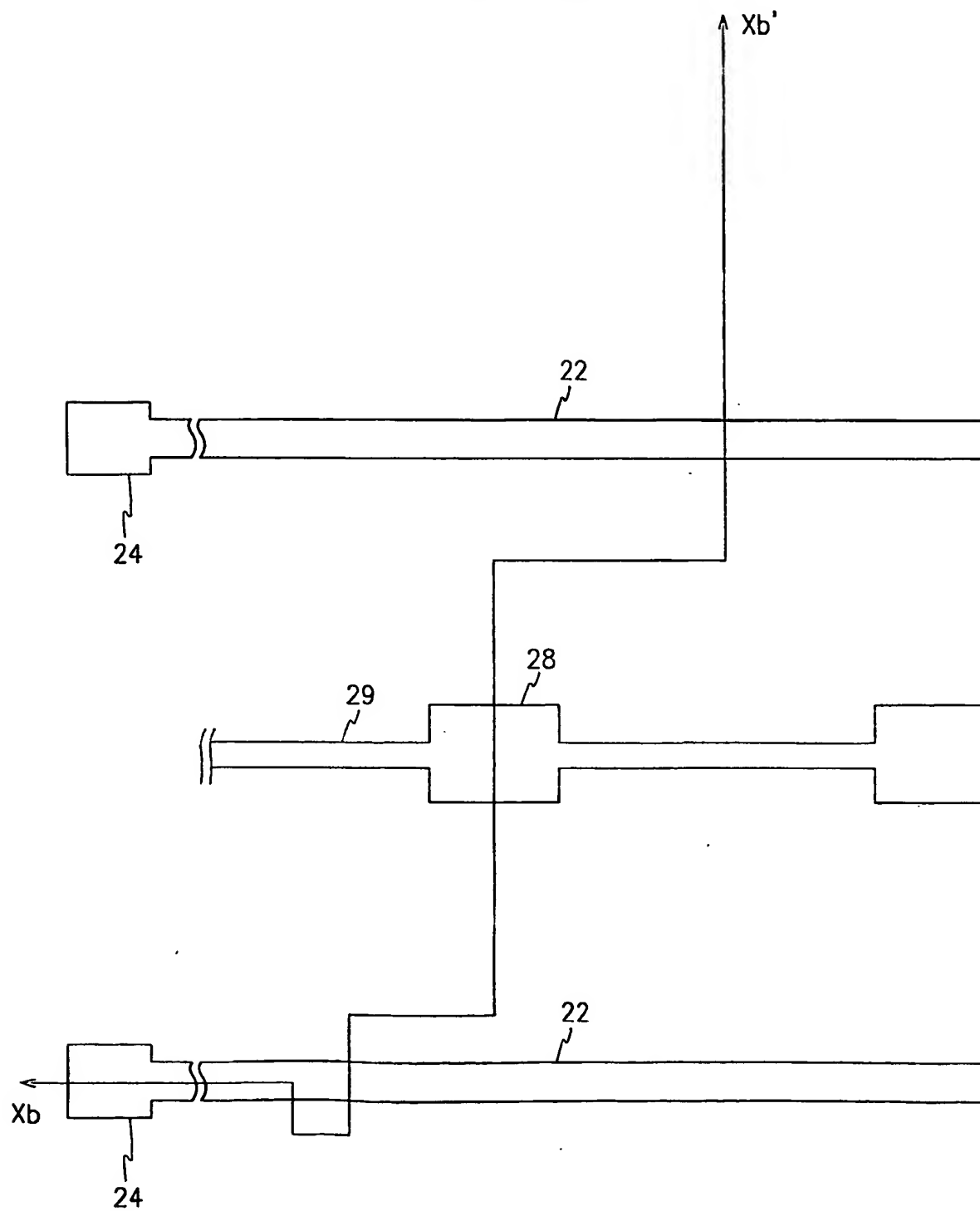
15/44

FIG. 9



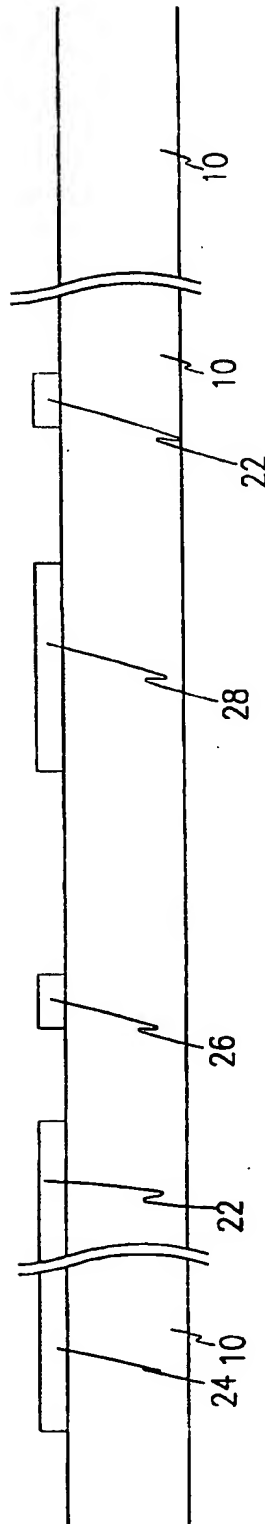
16/44

FIG.10a



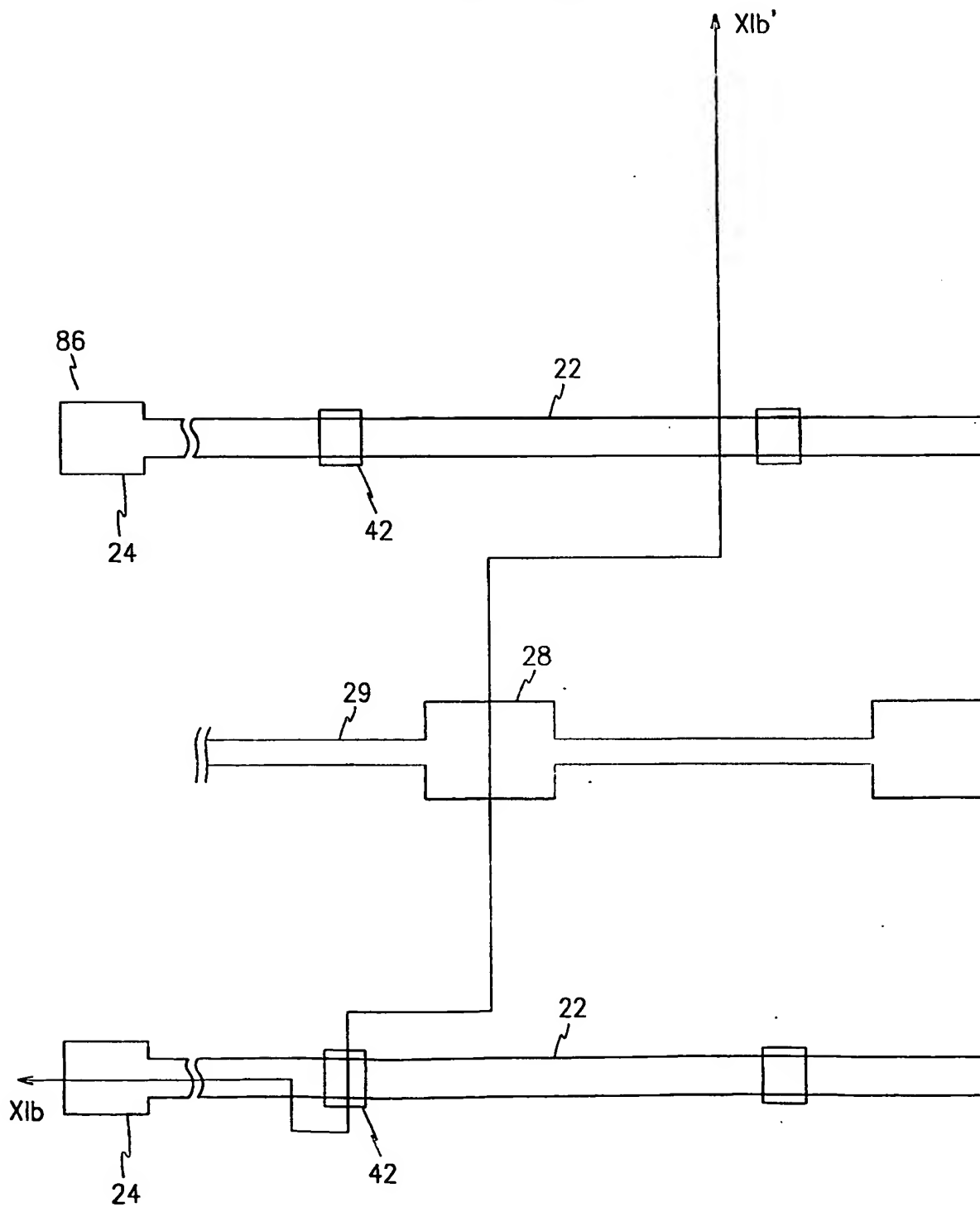
17/44

FIG.10b



18/44

FIG.11a



19/44

FIG.11b

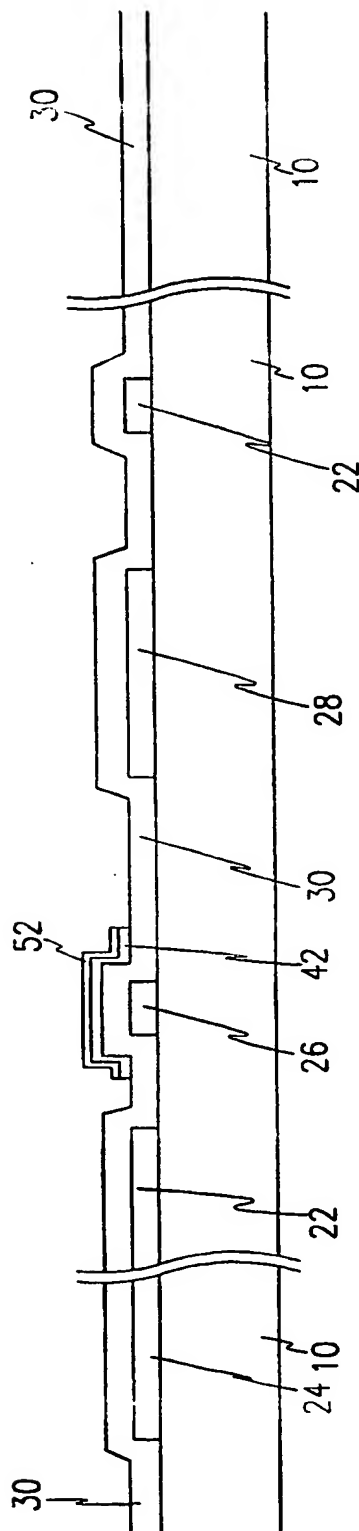
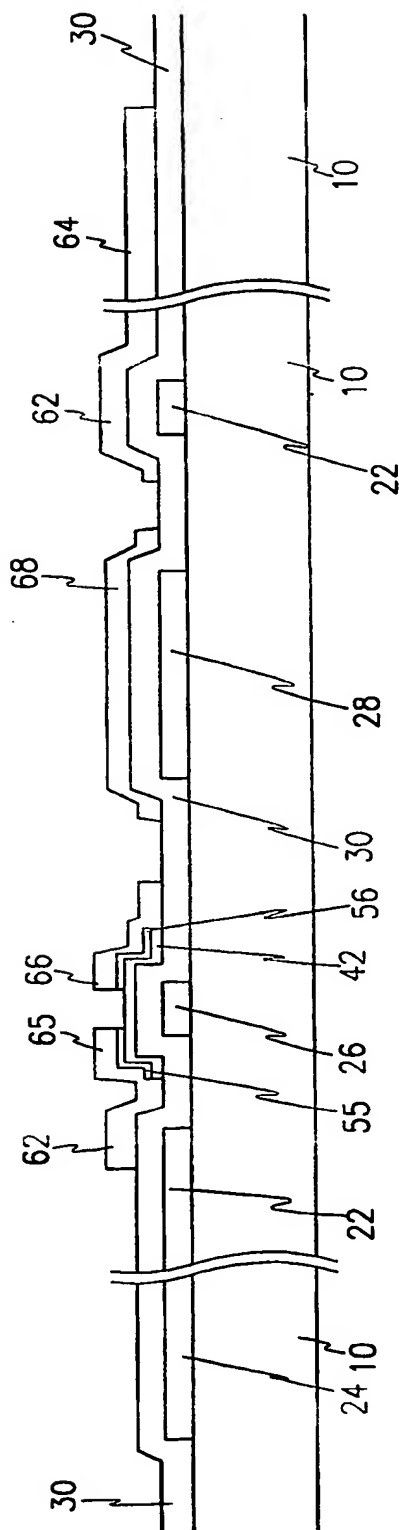
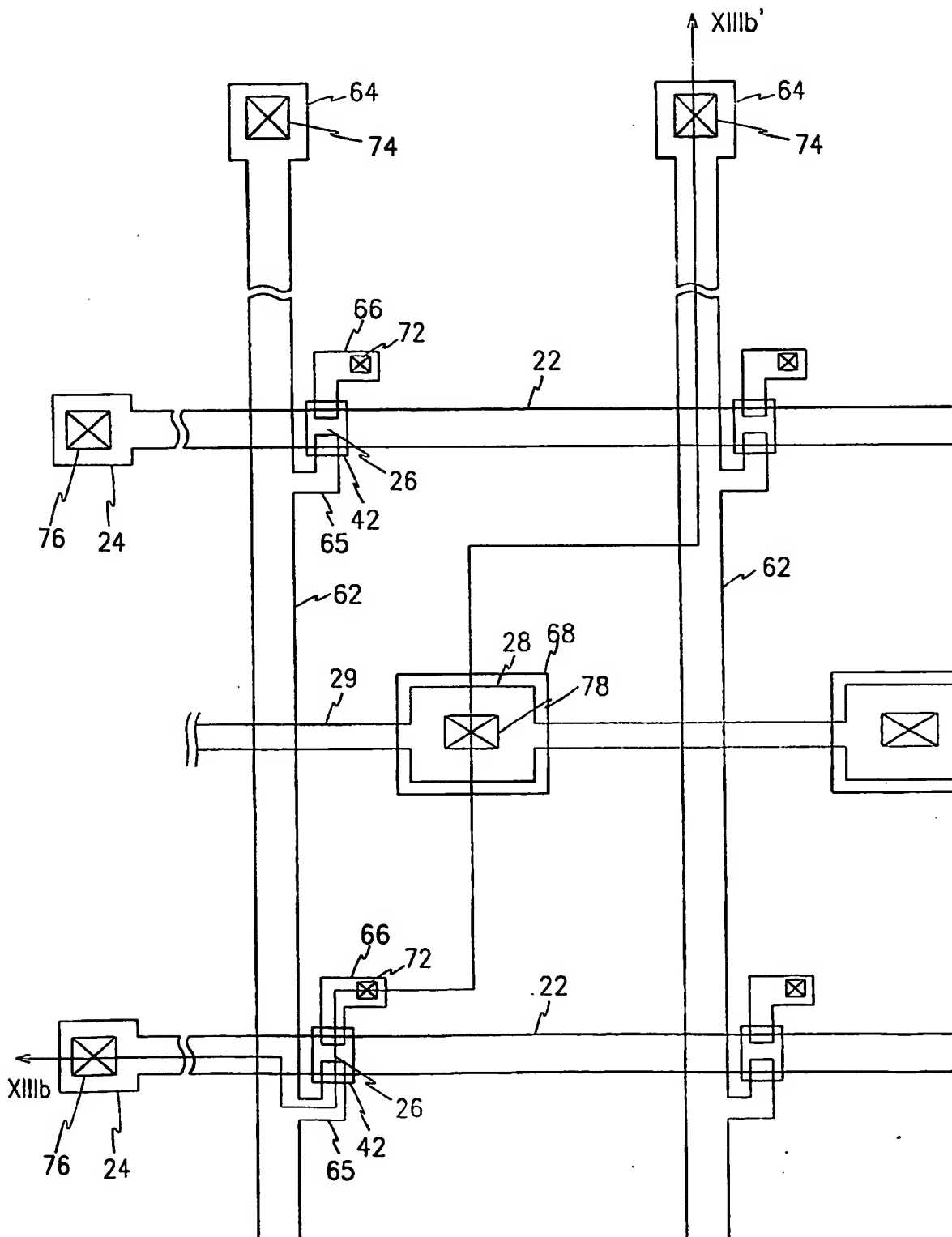


FIG.12b



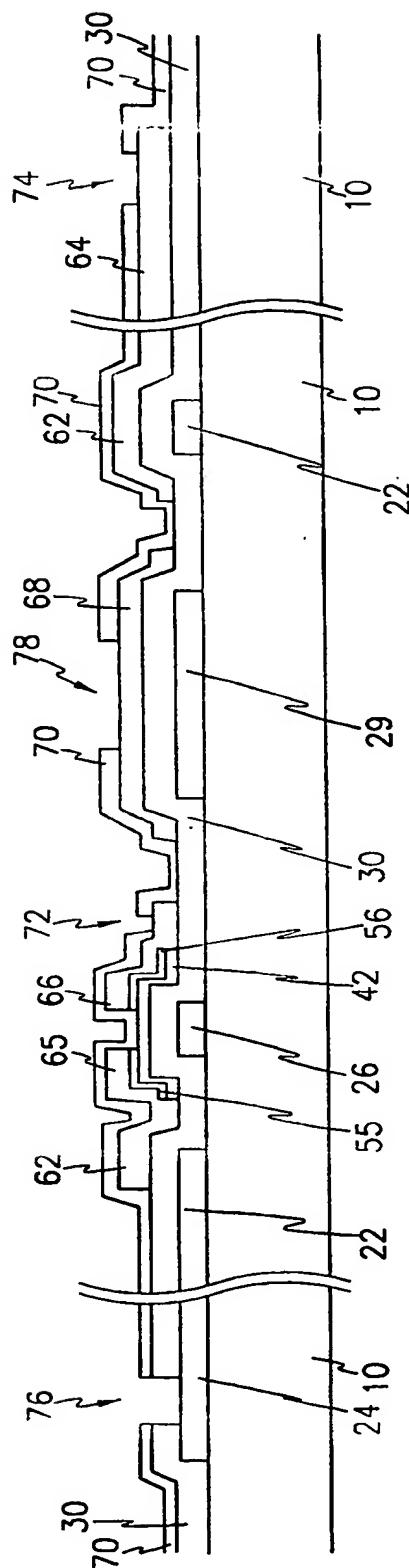
22/44

FIG.13a



23/44

FIG.13b



24/44

FIG.14

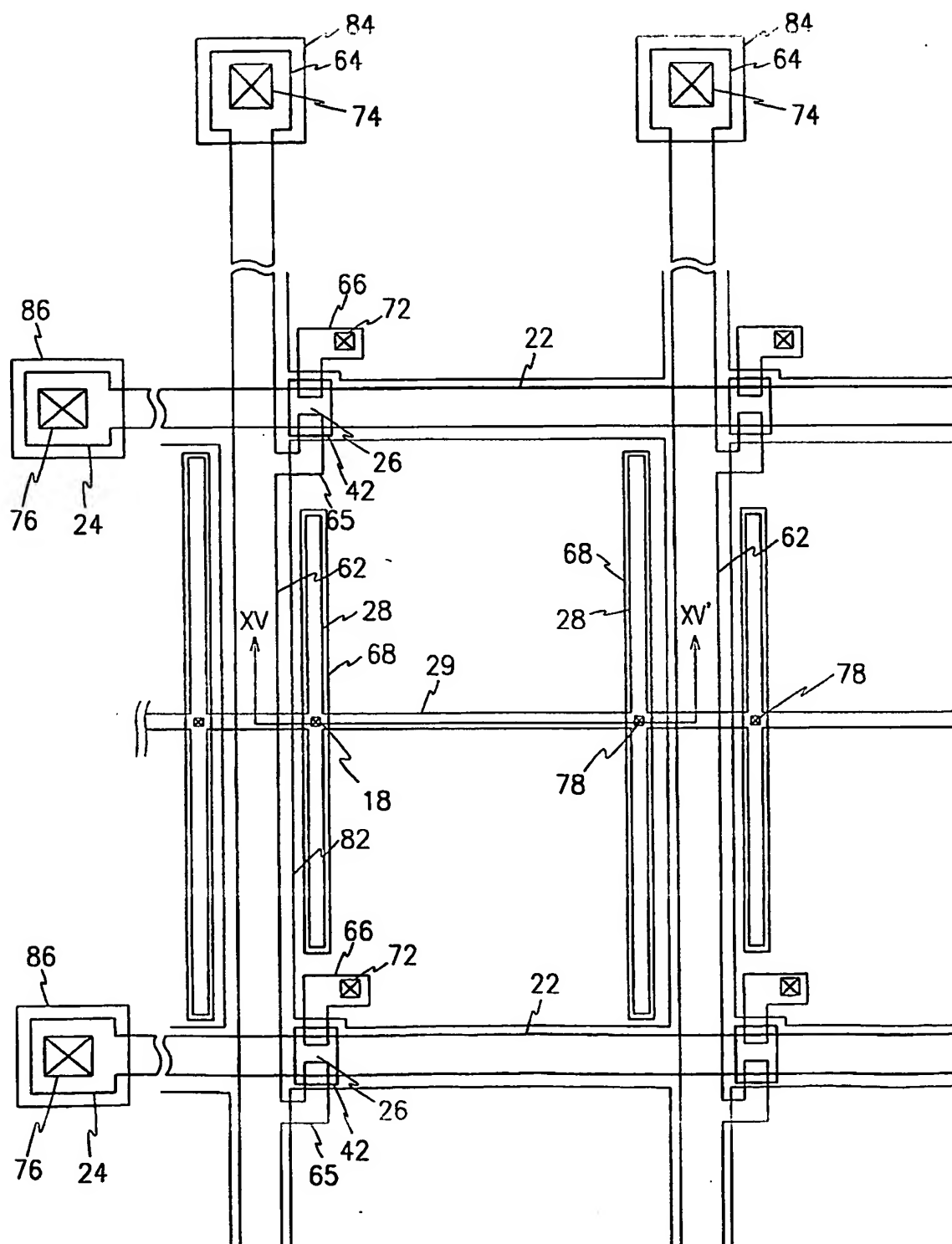
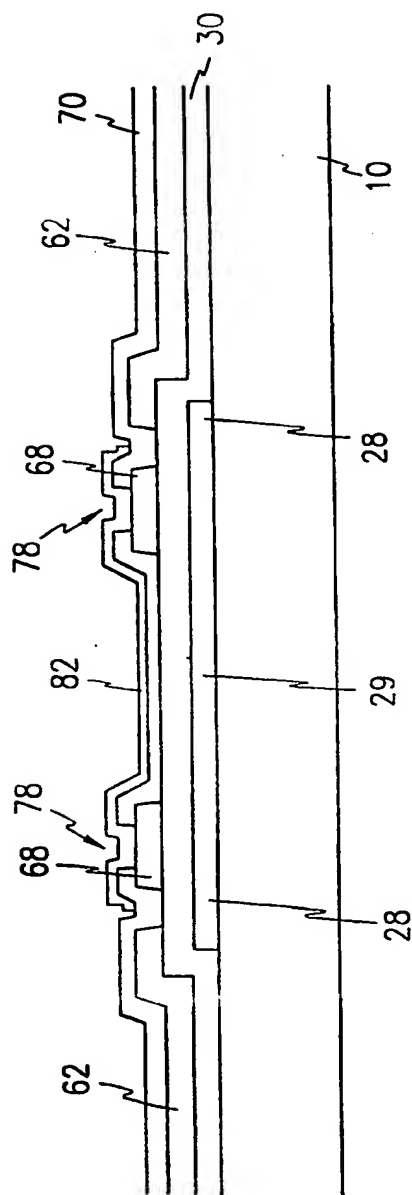
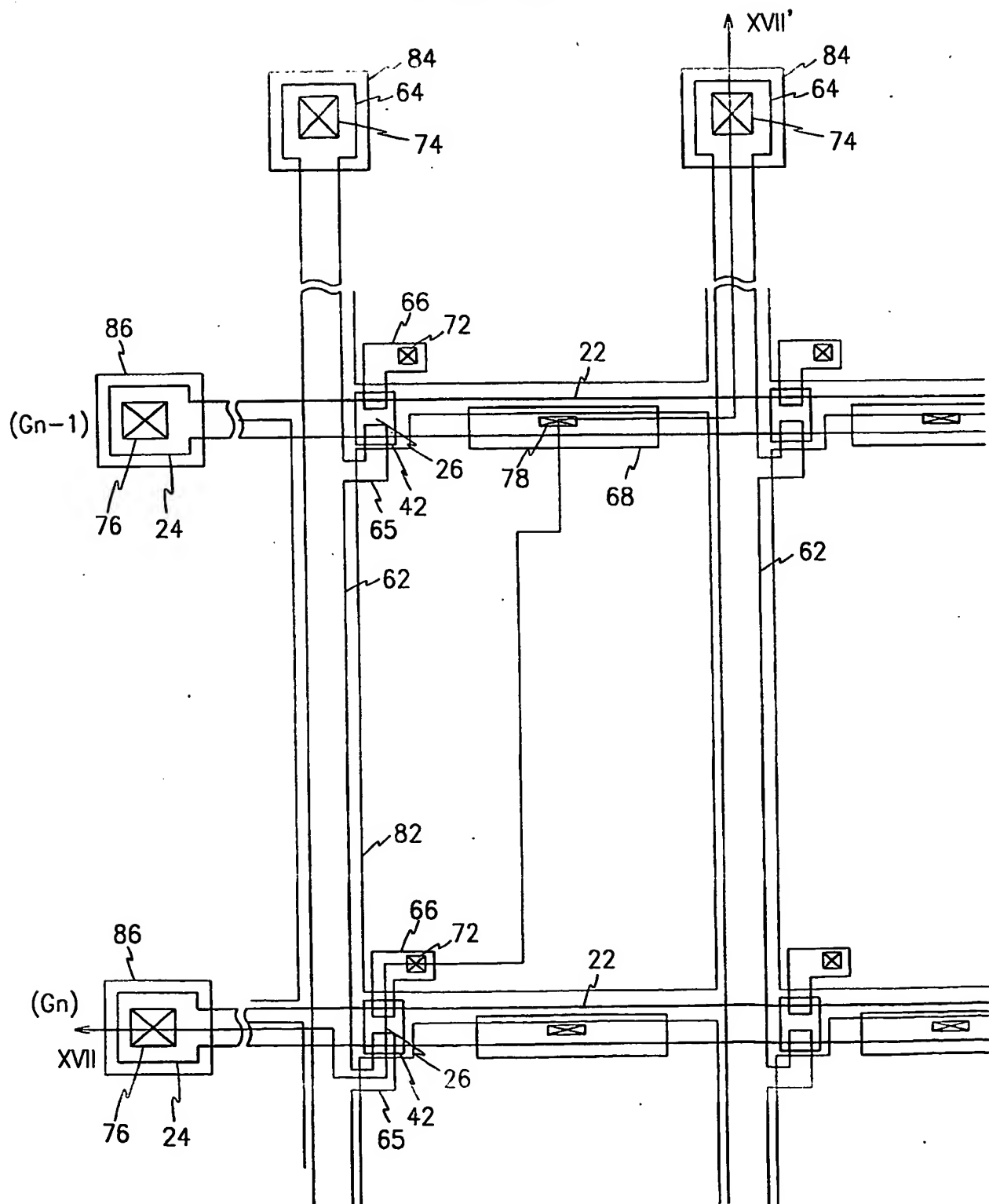


FIG.15



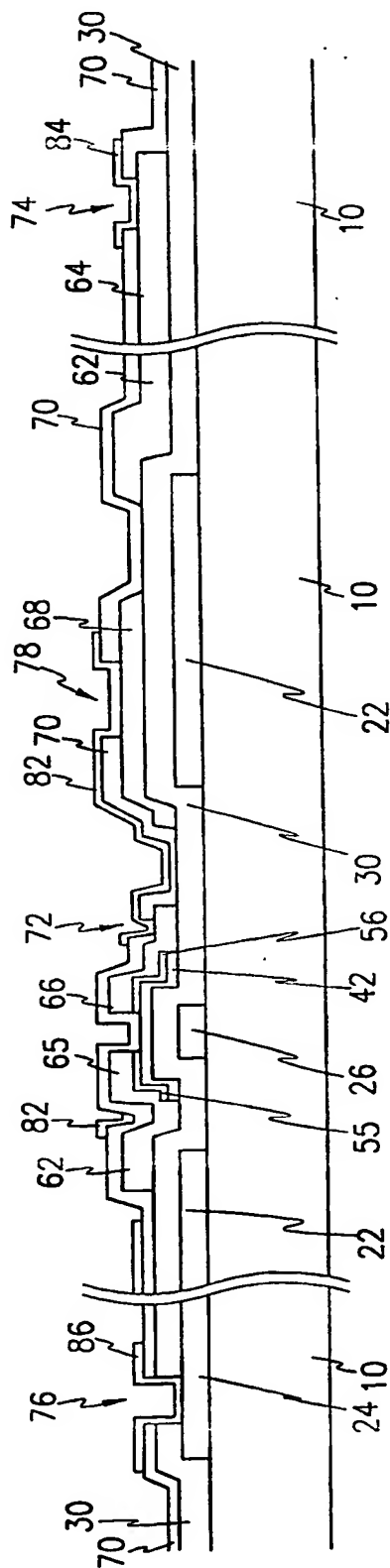
26/44

FIG.16



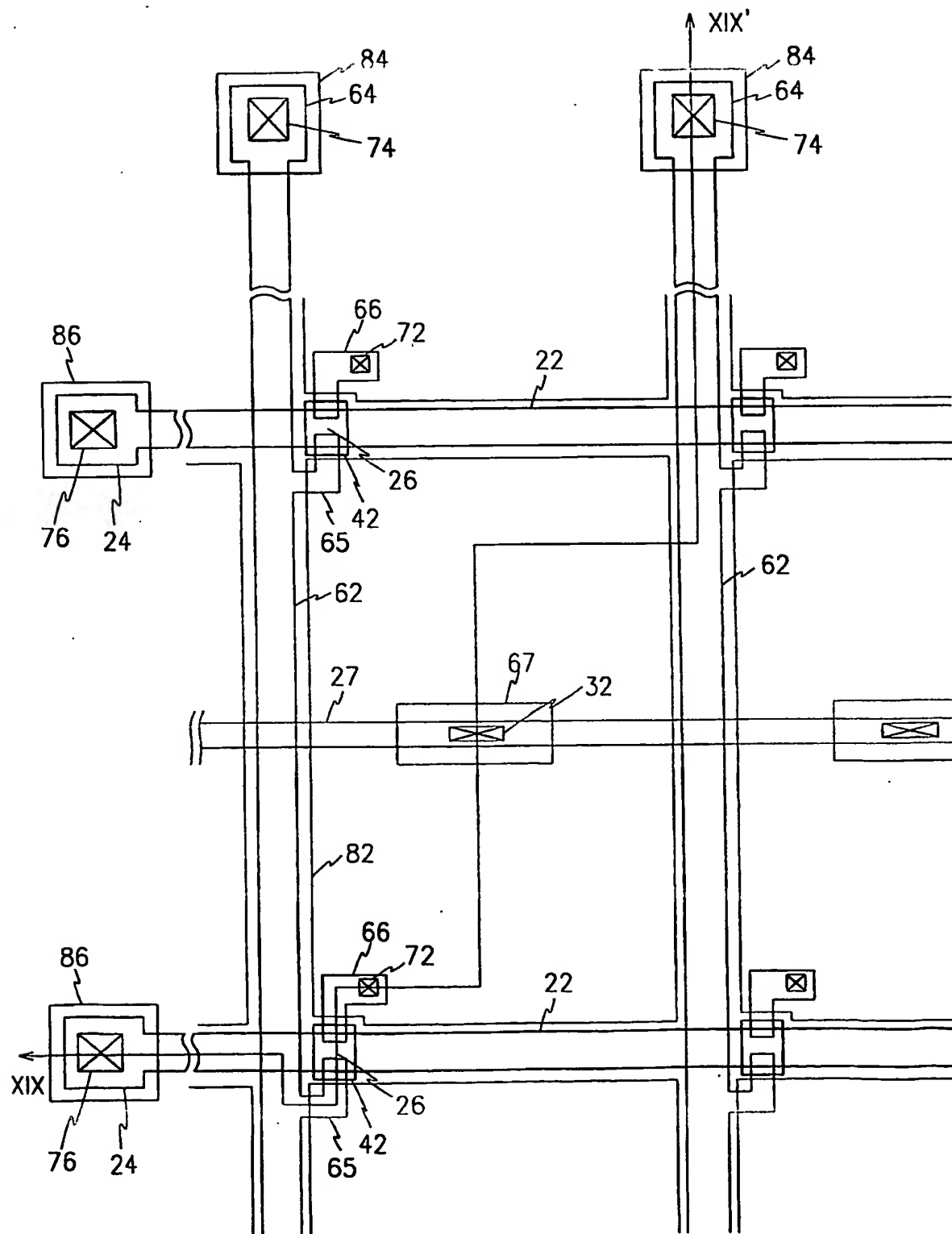
27/44

FIG.17



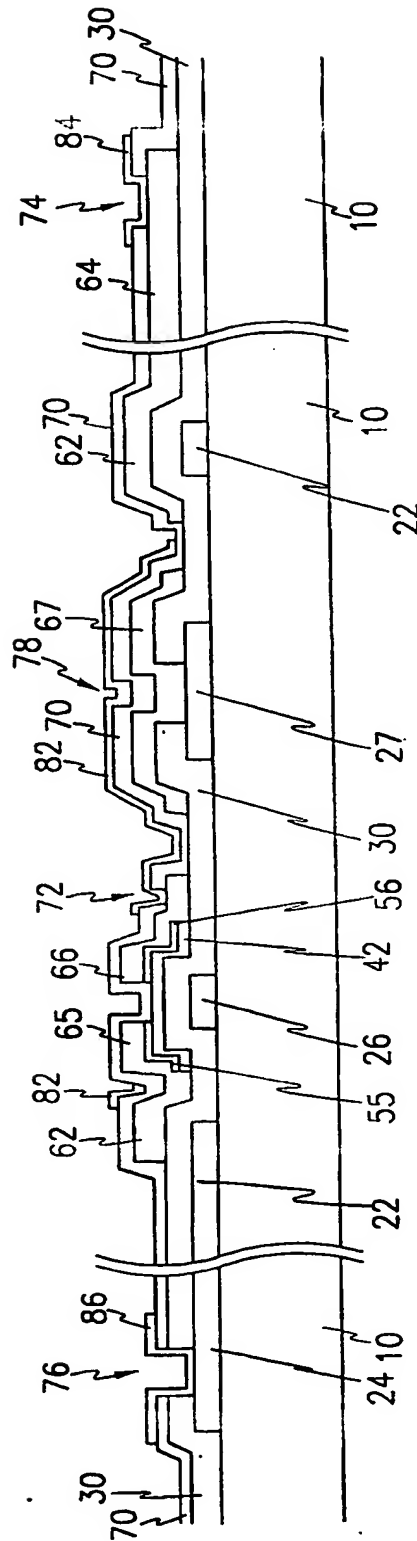
28/44

FIG.18



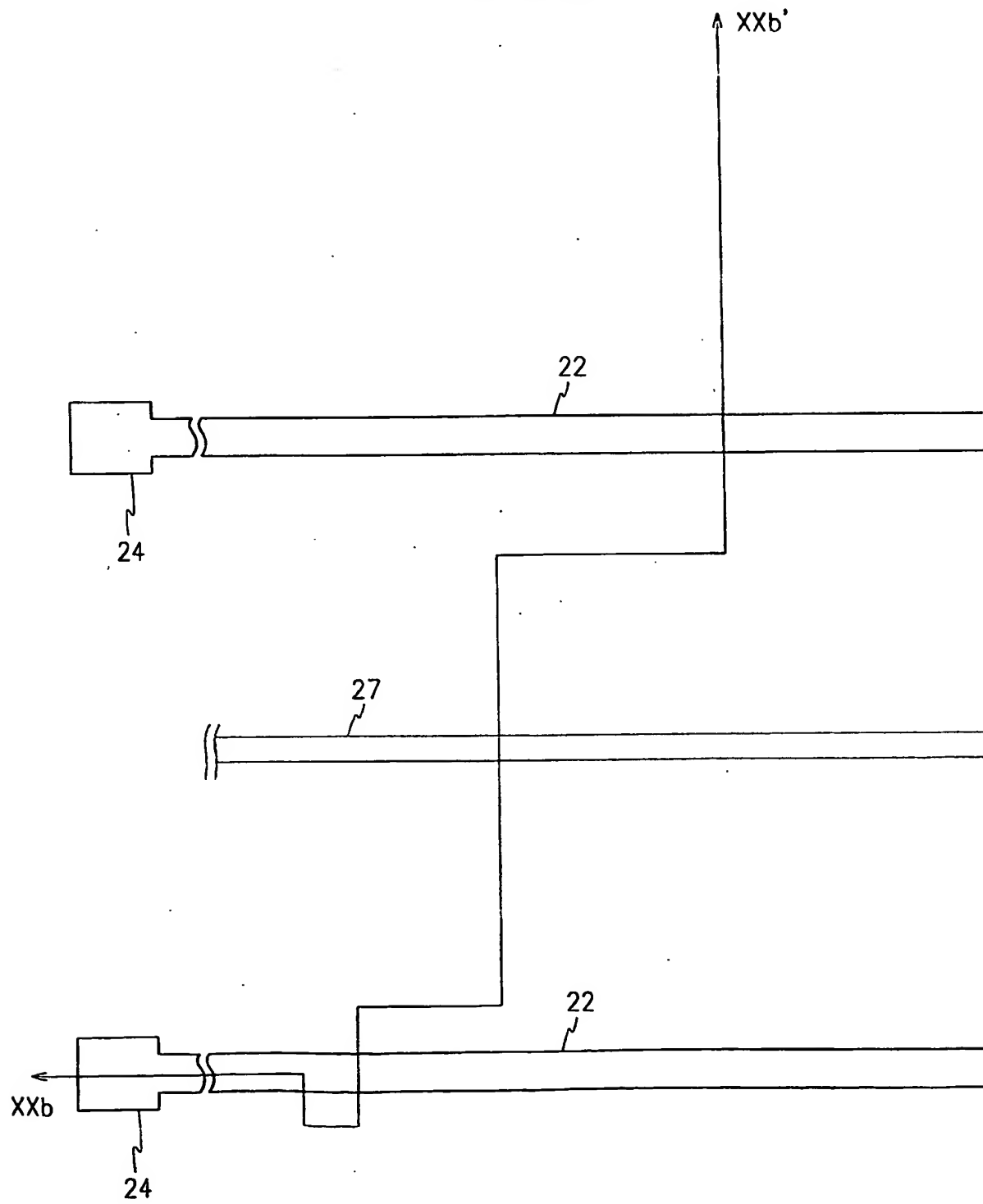
29/44

FIG.19



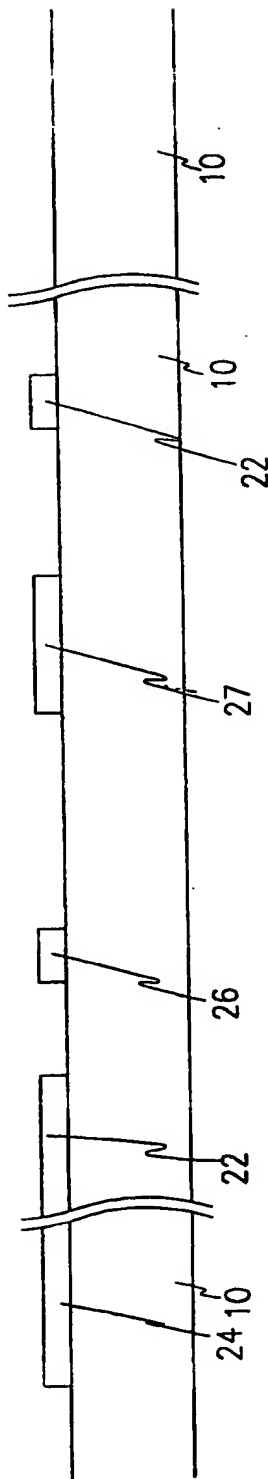
30/44

FIG.20a



31/44

FIG. 20b



32/44

FIG.21a

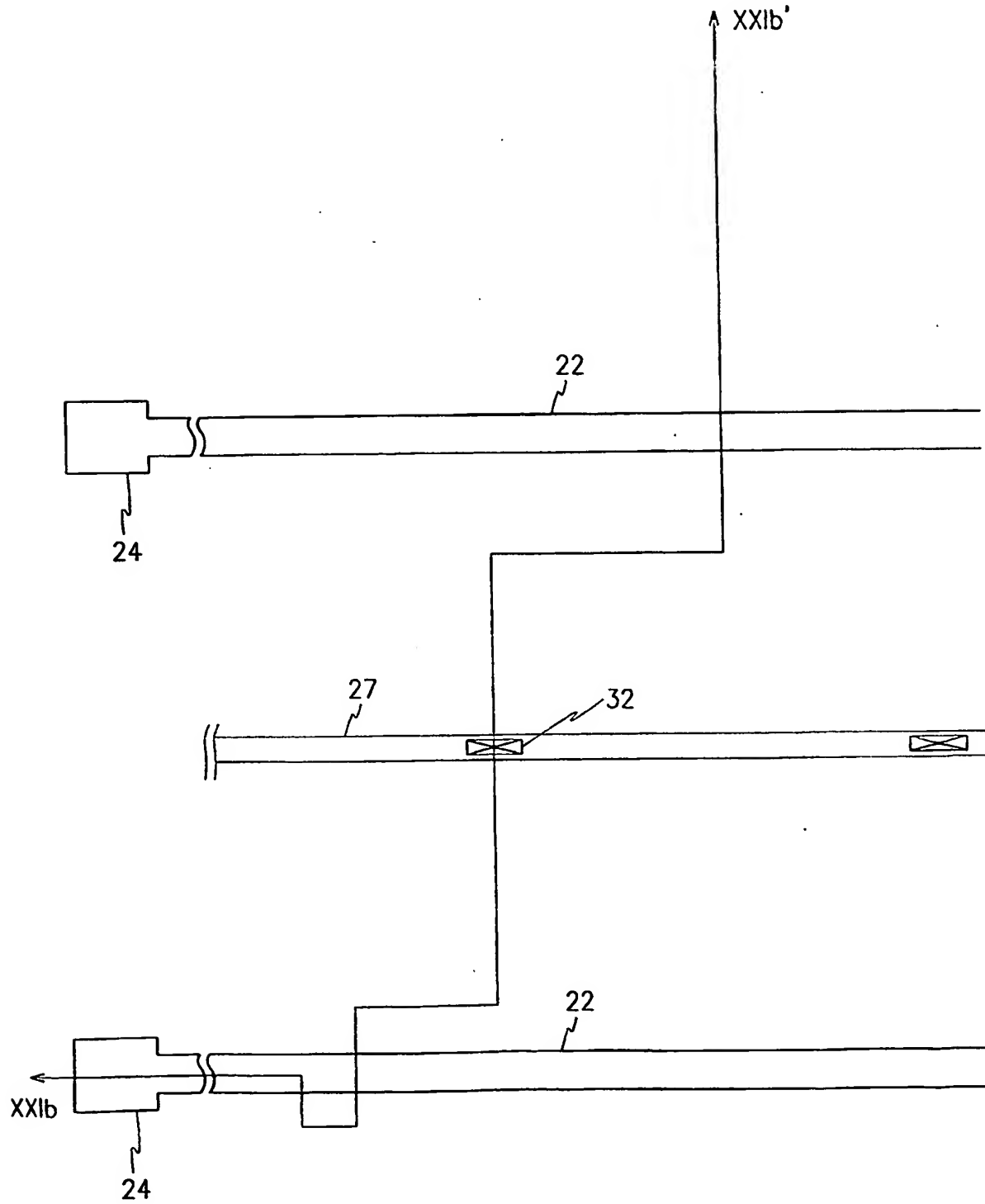
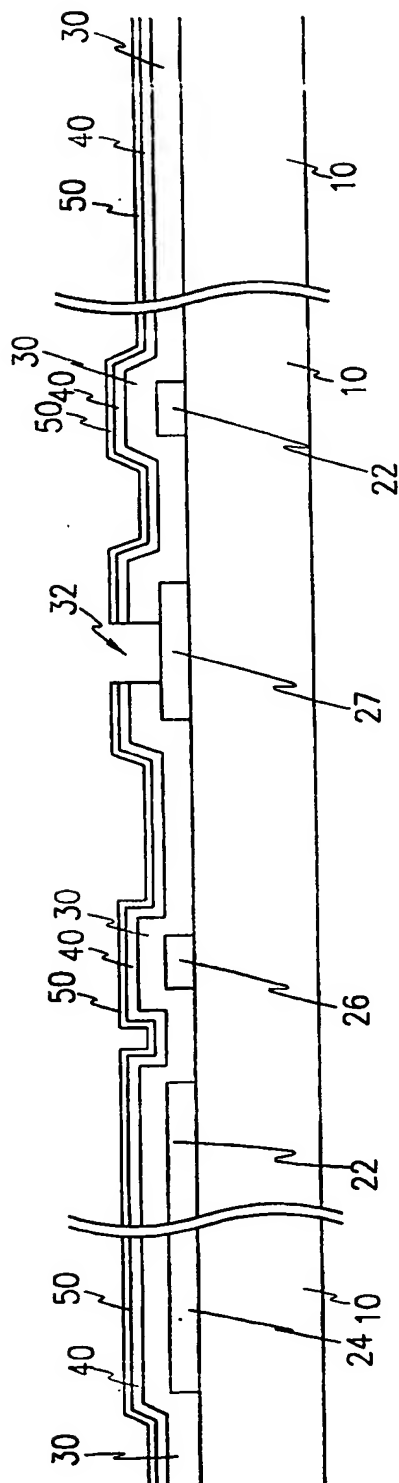


FIG. 21b



34/44

FIG. 22a

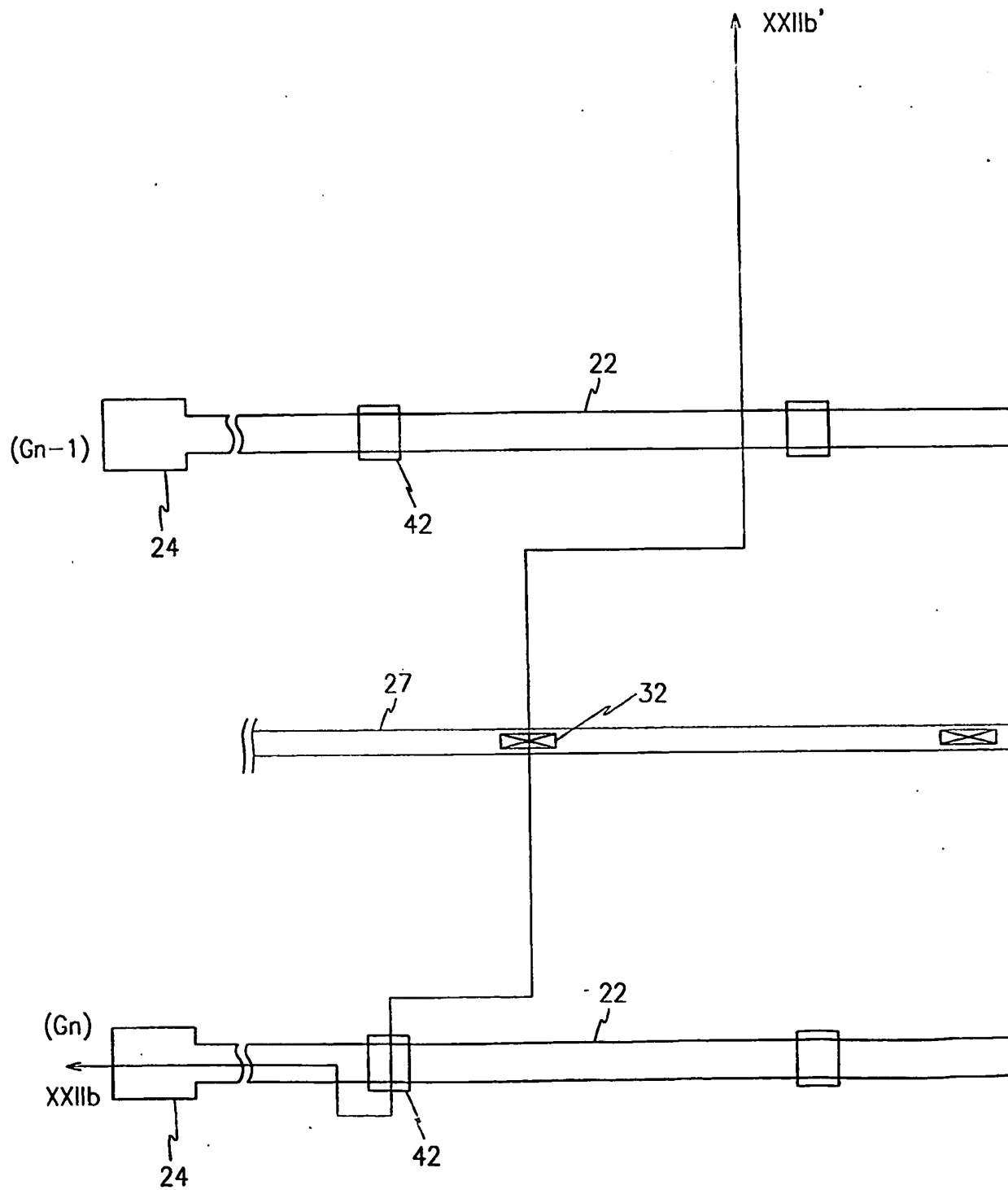
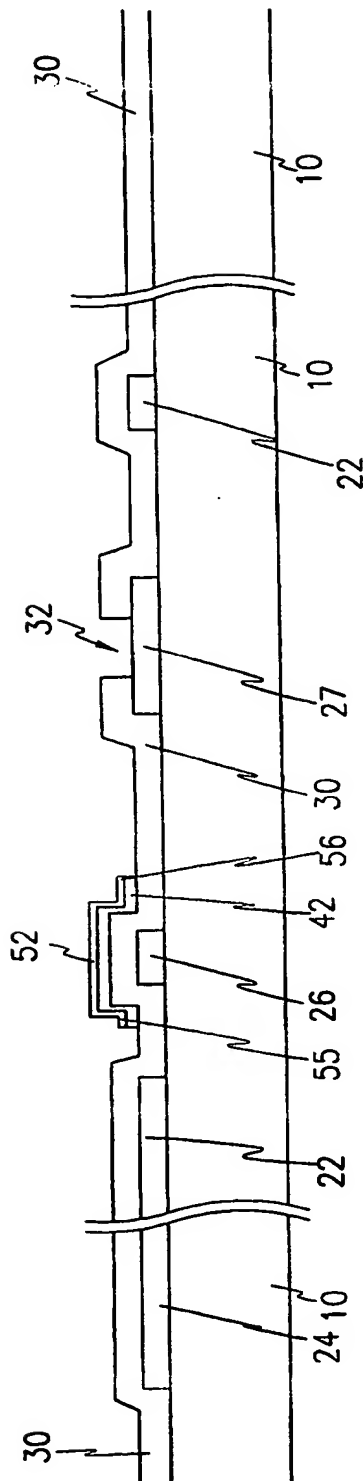


FIG. 22b



36/44

FIG.23a

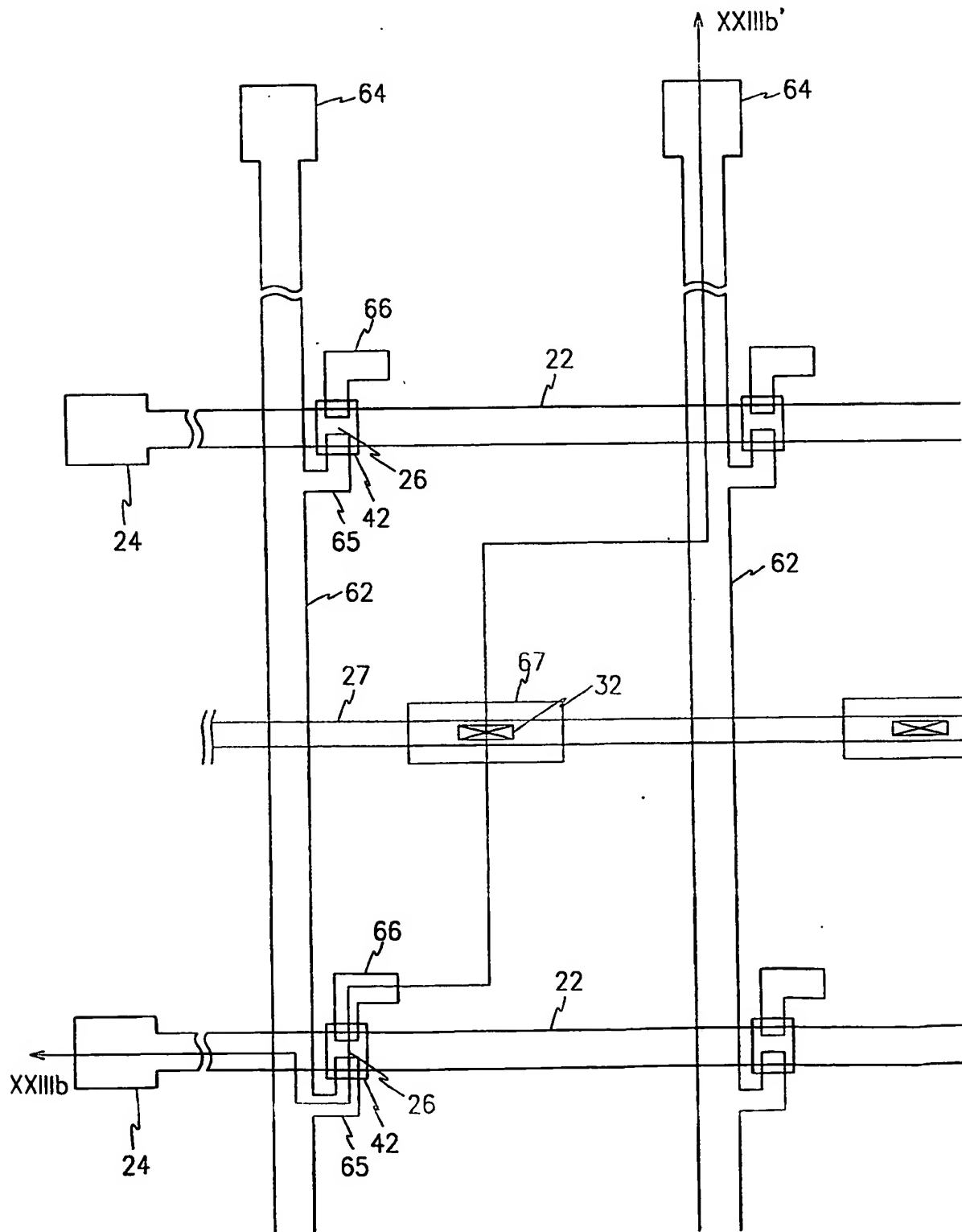
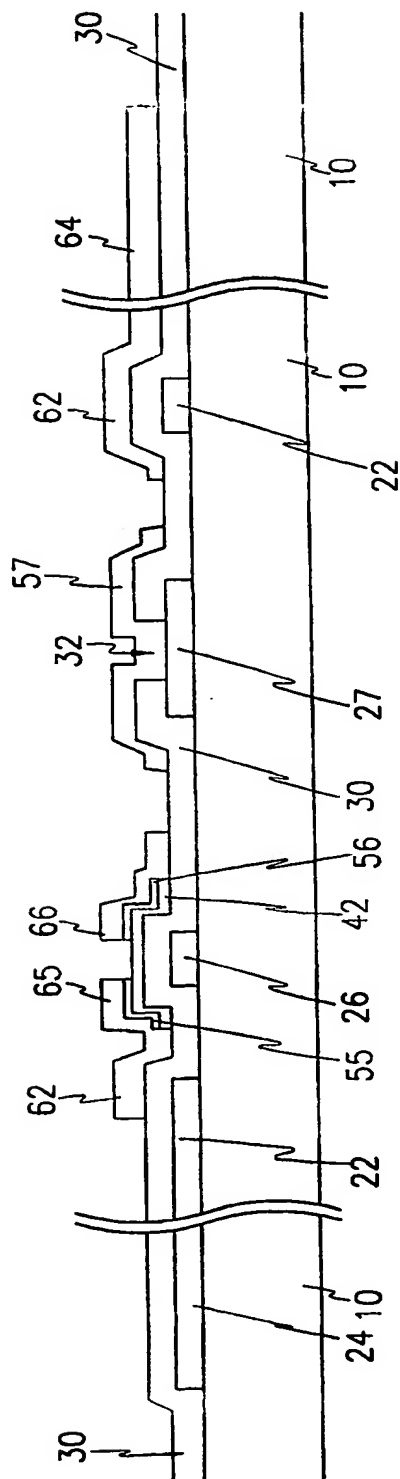
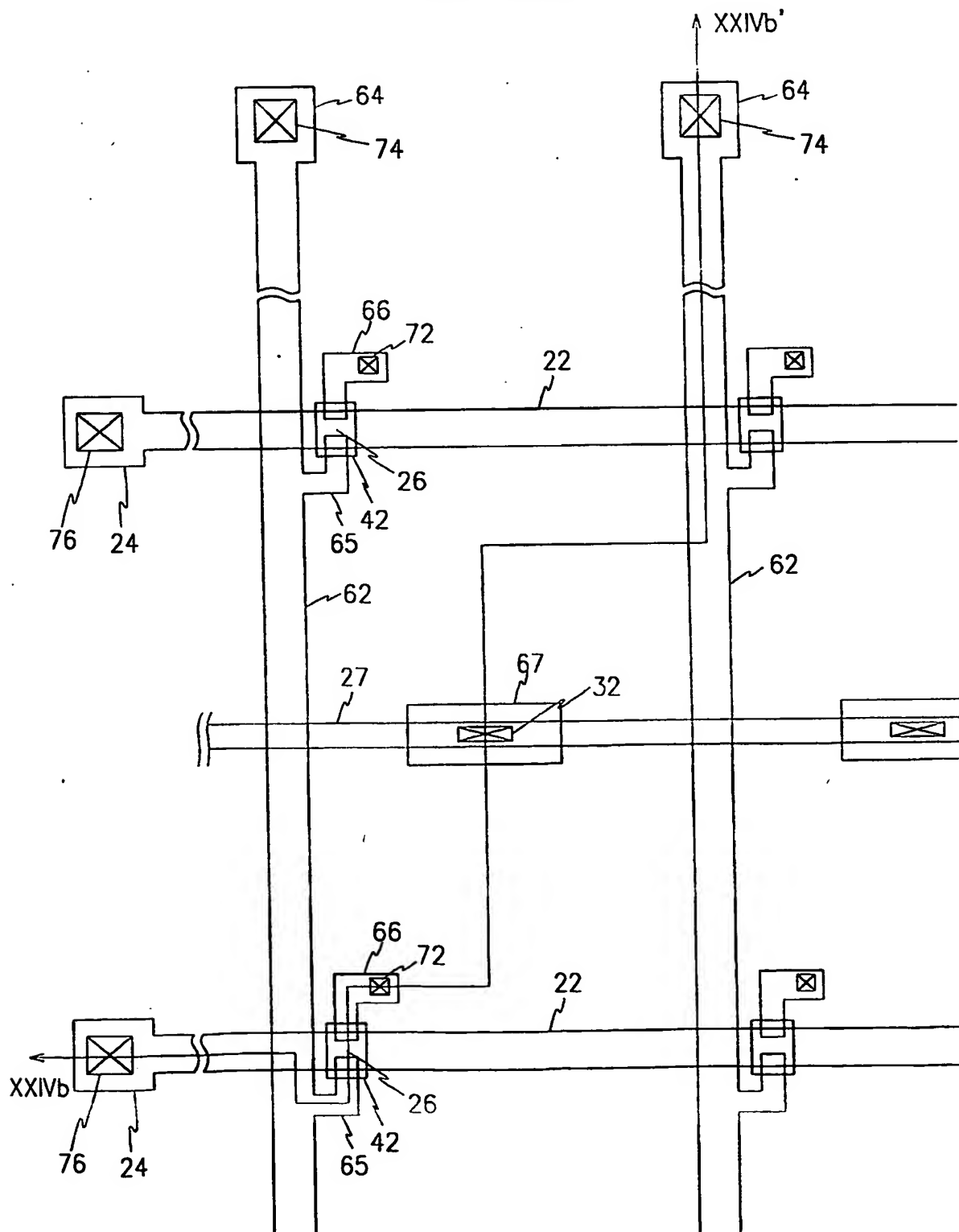


FIG. 23b



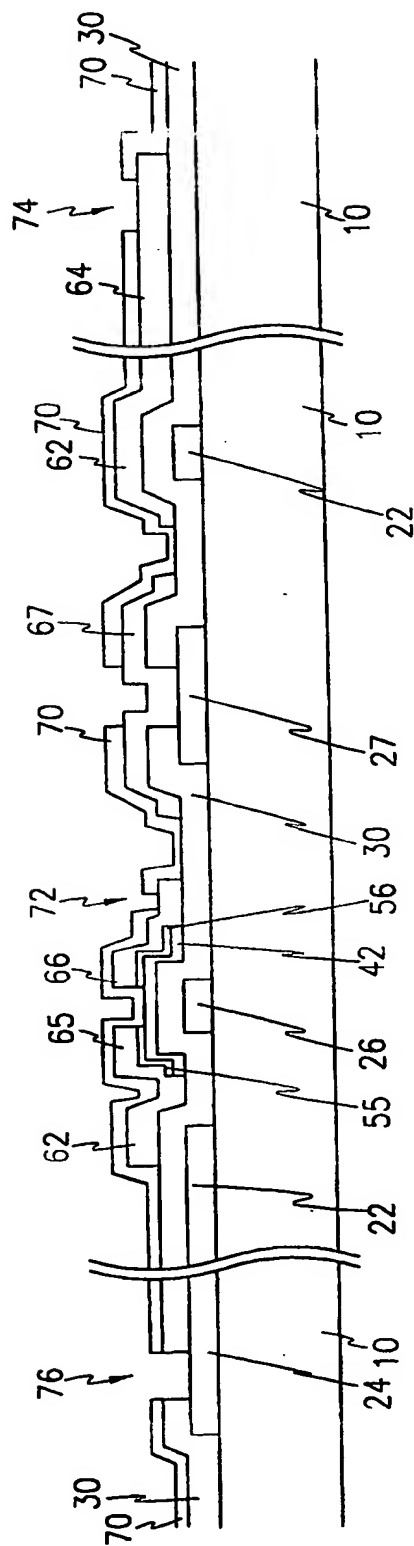
38/44

FIG. 24a



39/44

FIG. 24b



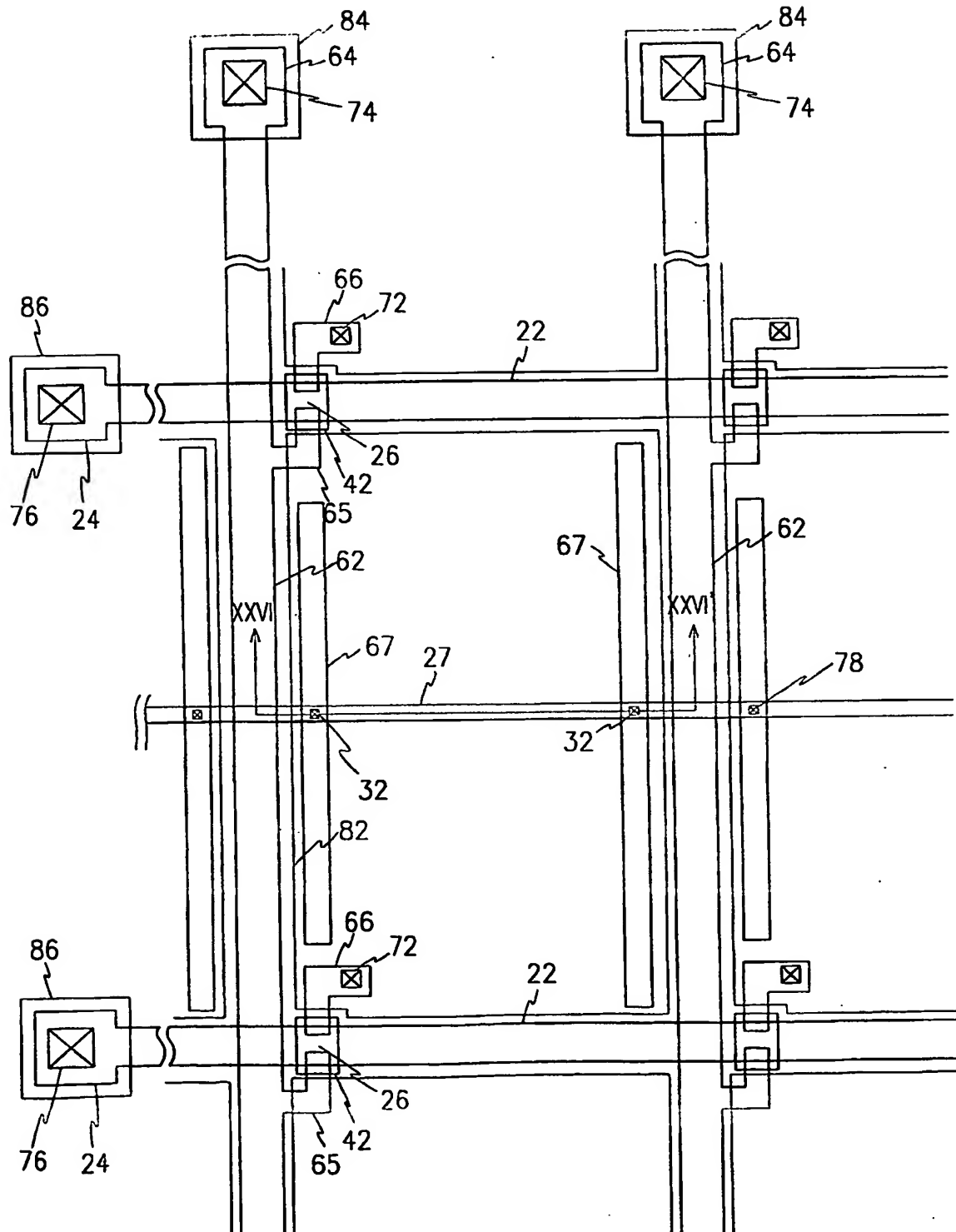
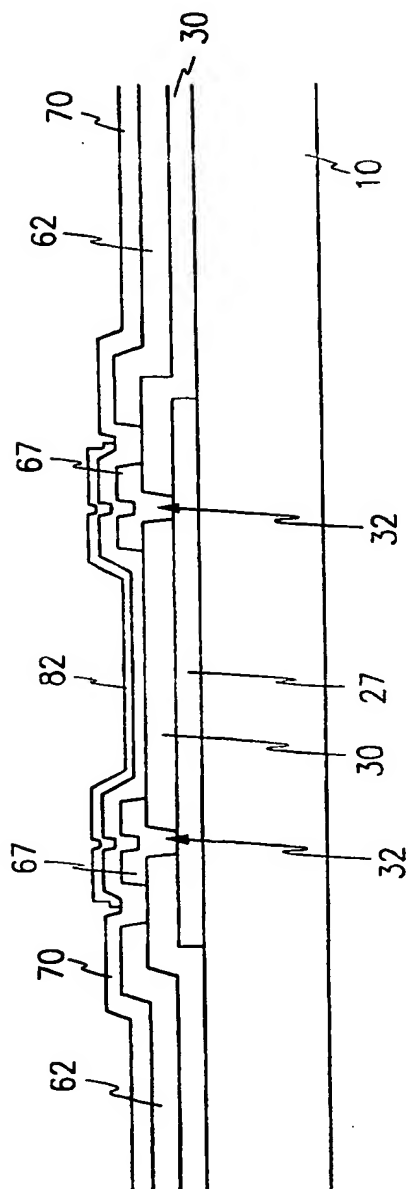
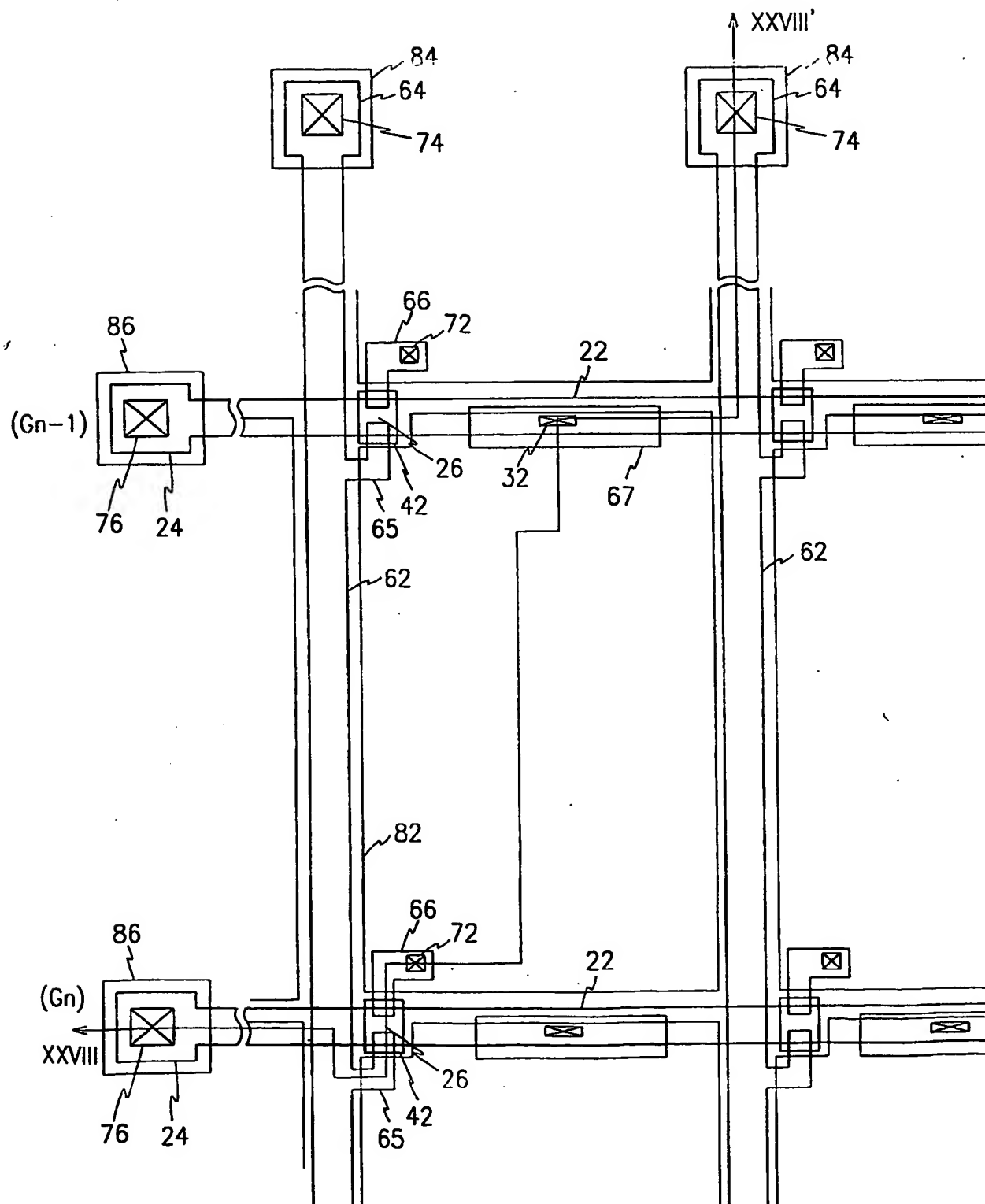
40/44
FIG.25

FIG. 26



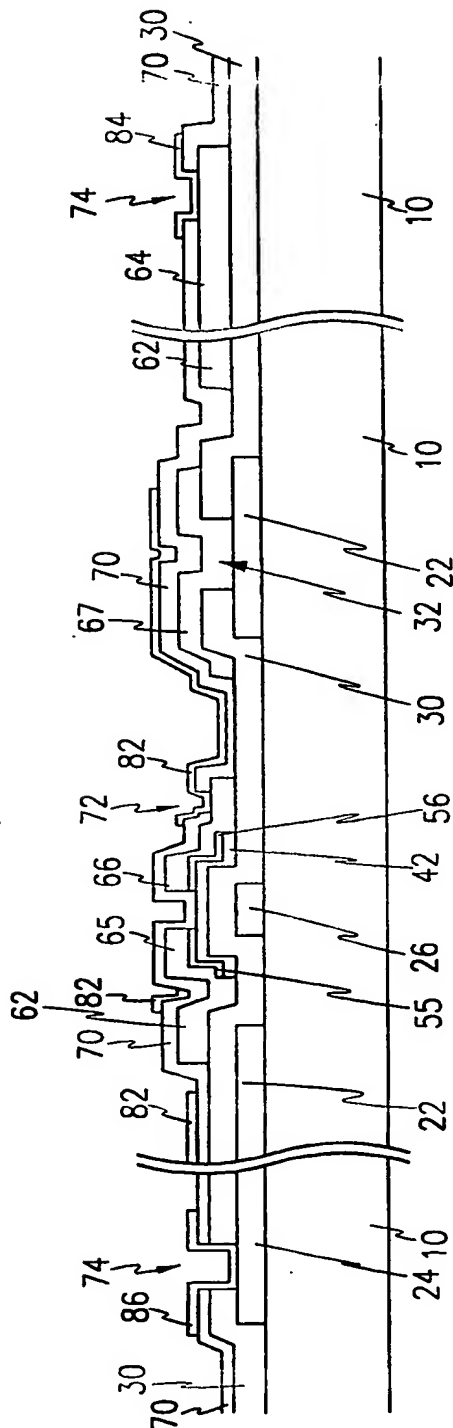
42/44

FIG.27



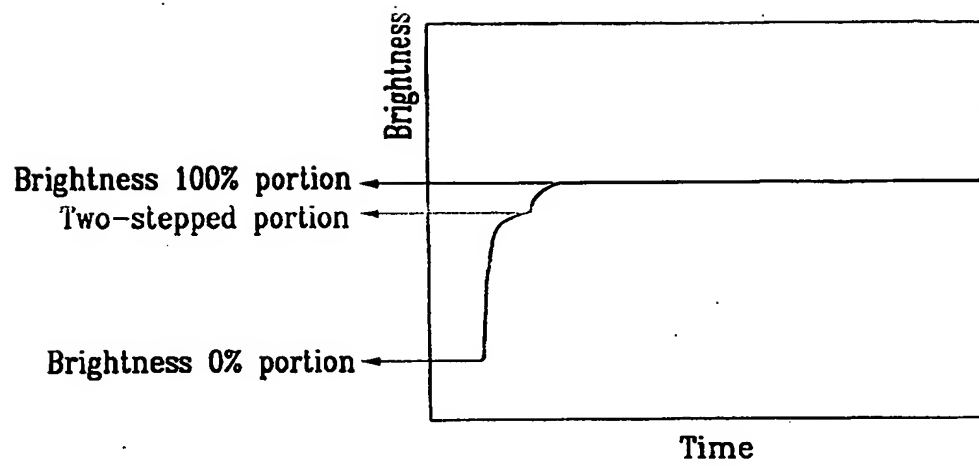
43/44

FIG.28



44/44

FIG.29



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR02/00334

A. CLASSIFICATION OF SUBJECT MATTER

IPC7 G02F 1/1343

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7 G02F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

eKIPASS

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

"crystal", "aperture", "storage", "pixel", etc.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	KR A 1997-007427(SAMSUNG ELECTRONICS CD.,LTD) 21-02-1997 see the whole paper	1
A	KR A 1995-029822(SAMSUNG ELECTRONICS CD.,LTD) 24-11-1995 see the whole paper	1-41
A	KR A 1996-002917(SAMSUNG ELECTRONICS CD.,LTD) 26-01-1996 see the whole paper	1-41

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
 "A" document defining the general state of the art which is not considered to be of particular relevance
 "E" earlier application or patent but published on or after the international filing date
 "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
 "O" document referring to an oral disclosure, use, exhibition or other means
 "P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
 "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
 "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
 "&" document member of the same patent family

Date of the actual completion of the international search

28 JANUARY 2003 (28.01.2003)

Date of mailing of the international search report

28 JANUARY 2003 (28.01.2003)

Name and mailing address of the ISA/KR



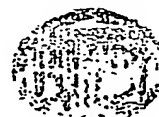
Korean Intellectual Property Office
920 Dunsan-dong, Seo-gu, Daejeon 302-701,
Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

PARK, Je Hyun

Telephone No. 82-42-481-5760



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/KR02/00334

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
KR A 1997-007427	21-02-1997	NONE	
KR A 1995-029822	24-11-1995	NONE	
KR A 1996-002917	26-01-1996	NONE	

INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR02/00334

A. CLASSIFICATION OF SUBJECT MATTER

IPC7 G02F 1/1343

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7 G02F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

eKIPASS

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

"crystal", "aperture", "storage", "pixel", etc.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	KR A 1997-007427(SAMSUNG ELECTRONICS CD.,LTD) 21-02-1997 see the whole paper	1
A	KR A 1995-029822(SAMSUNG ELECTRONICS CD.,LTD) 24-11-1995 see the whole paper	1-41
A	KR A 1996-002917(SAMSUNG ELECTRONICS CD.,LTD) 26-01-1996 see the whole paper	1-41

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family


Date of the actual completion of the international search

28 JANUARY 2003 (28.01.2003)

Date of mailing of the international search report

28 JANUARY 2003 (28.01.2003)

Name and mailing address of the ISA/KR

 Korean Intellectual Property Office
920 Dunsan-dong, Seo-gu, Daejeon 302-701,
Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

PARK, Je Hyun

Telephone No. 82-42-481-5760



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/KR02/00334

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
KR A 1997-007427	21-02-1997	NONE	
KR A 1995-029822	24-11-1995	NONE	
KR A 1996-002917	26-01-1996	NONE	